NX5DV715

Dual supply 1-of-2 VGA switch

Rev. 3 — 4 November 2011 Product data sheet

1. General description

The NX5DV715 is a dual supply 1-to-2 VGA switch. It integrates high-bandwidth SPDT switches with level-translating buffers and level translating switches to provide switching of input RGB, H-Sync, V-Sync and DDC signals to either of two output channels.

The NX5DV715 is characterized for operation from −40 °C to +85 °C.

2. Features and benefits

- RGB switches:
  - Low ON resistance (4 Ω typical)
  - Low ON capacitance (12 pF typical)
  - Low output skew (50 ps)
- Low power consumption (< 2 μA)
- Level translation of sync and DDC signals
- Over-voltage tolerant inputs
- ESD protection:
  - HBM JESD22-A114F Class 3A exceeds 4 kV
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101D exceeds 1000 V
  - IEC61000-4-2 contact discharge exceeds 4 kV for I/Os
- Specified from −40 °C to +85 °C

3. Applications

- Notebook Computers
- Docking stations
- Digital projectors
- Computer monitors
- Servers
- Storage

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NX5DV715HF	−40 °C to +85 °C	HWQFN32	plastic thermal enhanced very very thin quad flat package; no leads; 32 terminals; body 3 × 6 × 0.75 mm	SOT1180-1

5. Functional diagram

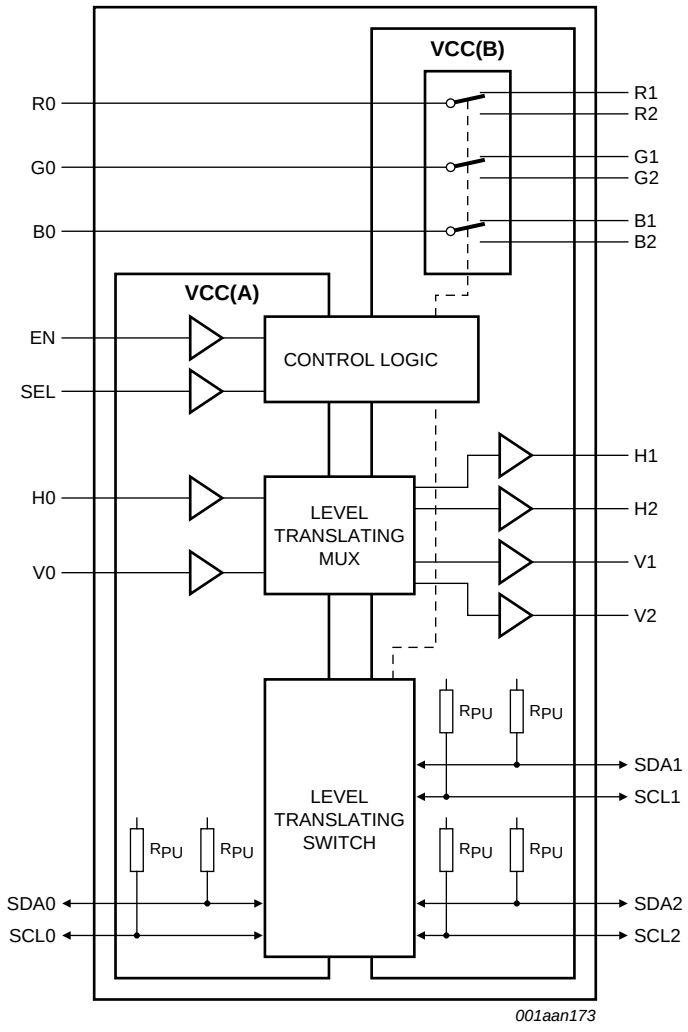
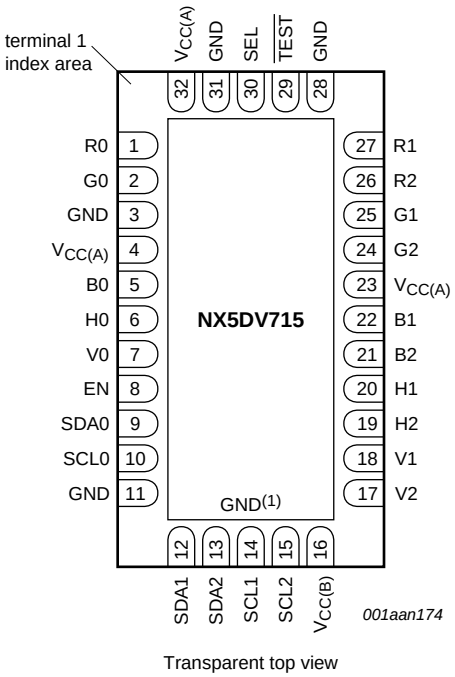


Fig 1. Logic symbol

6. Pinning information

6.1 Pinning



Transparent top view

(1) This is not a supply pin, the substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad however if it is soldered the solder land should remain floating or be connected to GND.

Fig 2. Pin configuration SOT1180-1 (HWQFN32)

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
R0, G0, B0	1, 2, 5	RGB input or output
GND	3, 11, 28, 31	ground (0 V)
$V_{CC(A)}$	4, 23, 32	supply voltage A
H0	6	horizontal sync input
V0	7	vertical sync input
EN	8	enable input (active HIGH)
SDA0	9	SDA0 input or output
SCL0	10	SCL0 input or output
SDA1, SDA2	12, 13	SDA input or output
SCL1, SCL2	14, 15	SCL input or output
$V_{CC(B)}$	16	supply voltage B
V1, V2	18, 17	vertical sync output
H1, H2	20, 19	horizontal sync output

Table 2. Pin description *...continued*

Symbol	Pin	Description
R1, G1, B1, R2, G2, B2	27, 25, 22, 26, 24, 21	RGB input or output
$\overline{\text{TEST}}$[1]	29	test pin (active LOW)
SEL	30	select input

[1] Test pin used to enable test mode. For normal usage, this pin must be connected to $V_{CC(A)}$.

7. Functional description

The NX5DV715 integrates high-bandwidth SPDT switches, level-translating buffers and level translating SPDT switches to provide a complete solution for 1-to-2 switching of VGA signals. An enable input (EN) is used to enable or disable the device and a select input (SEL) is used to determine which output is selected. When EN = LOW the device is disabled; all switches will be off, pull-up resistors will be disabled and H1, V1, H2, V2 will be forced LOW.

7.1 RGB switches

The NX5DV715 provides three identical single pole double throw high-bandwidth switches to route standard VGA RGB signals (see Table 3).

Table 3. Function table RGB

H = HIGH voltage level; L = LOW voltage level; X = Don't care.

Input		Switch
EN	SEL	
H	L	R0 to R1; G0 to G1; B0 to B1
H	H	R0 to R2; G0 to G2; B0 to B2
L	X	switches Rn, Gn, Bn off

7.2 H-Sync/V-Sync level translator

The horizontal and vertical synchronization buffers have inputs (H0, V0) referenced to $V_{CC(A)}$ and outputs (H1, V1 and H2, V2) that are referenced to $V_{CC(B)}$. This allows level translation of synchronization signals from as low as 2.0 V up to 5.5 V and supports low-voltage CMOS or TTL-compatible graphics controllers meeting the VESA specification for output drive of ±8 mA. The EN input also controls the level shifter (See Table 4).

Table 4. Function table HV

H = HIGH voltage level; L = LOW voltage level; X = Don't care.

Input		Switch
EN	SEL	
H	L	H1 = H0; V1 = V0; H2, V2 = L
H	H	H2 = H0; V2 = V0; H1, V1 = L
L	X	L

7.3 Display-Data Channel Multiplexer

The NX5DV715 provides two identical SPDT active-level translating switches to route DDC signals (See Table 5). The switch outputs are limited to a diode drop less than the voltage applied on $V_{CC(A)}$. To provide VESA I^2C-compatible signals 3.3 V should be applied to $V_{CC(A)}$. If voltage translation is not required $V_{CC(A)}$ should be connected to $V_{CC(B)}$. Switch terminals include integrated pull-up resistors; inputs (SDA0, SCL0) are pulled up to $V_{CC(A)}$, outputs (SDA1, SCL1 and SDA2, SCL2) are pulled up to $V_{CC(B)}$. When the NX5DV715 is disabled (EN = LOW), the pull-up resistors are also disabled.

Table 5. Function table DDC

H = HIGH voltage level; L = LOW voltage level; X = Don't care.

Input		Switch
EN	**SEL**	
H	L	SDA0 to SDA1, SCL0 to SCL1
H	H	SDA0 to SDA2, SCL0 to SCL2
L	X	switches SDAn, SCLn off

8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(A)}$	supply voltage A			–0.5	+6	V
$V_{CC(B)}$	supply voltage B			–0.5	+6	V
V_I	input voltage		[1]	–0.5	+6	V
V_{SW}	switch voltage		[1]	–0.5	+6	V
I_{IK}	input clamping current	V_I < –0.5 V		–50	-	mA
I_{SK}	switch clamping current	V_I < –0.5 V		–50	-	mA
I_{OK}	output clamping current	V_O < 0 V		–50	-	mA
I_O	output current	V_O = 0 V to $V_{CC(B)}$		-	±50	mA
I_{CC}	supply current	$I_{CC(A)}$ or $I_{CC(B)}$		-	100	mA
I_{GND}	ground current			–100	-	mA
I_{SW}	switch current	V_{SW} > –0.5 V or V_{SW} < 6 V; source or sink current		-	±30	mA
		V_{SW} > –0.5 V or V_{SW} < 6 V; pulsed at 1 ms duration, < 10 % duty cycle; peak current		-	±90	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +85 °C	[2]	-	250	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] For HWQFN32 package: above 137 °C the value of P_{tot} derates linearly with 20.5 mW/K.

9. Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{CC(A)}$	supply voltage A			2	3.3	5.5	V
$V_{CC(B)}$	supply voltage B			4.5	5.0	5.5	V
T_{amb}	ambient temperature	operating in free-air		−40	+25	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC(A)}$ = 2.3 V to 2.7 V	[1]	-	20	-	ns/V
		$V_{CC(A)}$ = 3 V to 3.6 V	[1]	-	10	-	ns/V
		$V_{CC(A)}$ = 4.5 V to 5.5 V	[1]	-	5	-	ns/V

[1] Applies to control signal levels.

10. Static characteristics

Table 8. Static characteristics

$V_{CC(B)}$ = 4.5 V to 5.5 V; $V_{CC(A)}$ = 2 V to 5.5 V, unless otherwise specified; Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	T_{amb} = −40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
General						
$I_{CC(A)}$	supply current A	$V_{CC(A)}$ = 3.3 V; EN = $V_{CC(A)}$ or GND; for H1, H2, V1, V2: I_O = 0 A; SCLn, SDAn unconnected	-	-	2.0	µA
$I_{CC(B)}$	supply current B	$V_{CC(B)}$ = 5.0 V; EN = $V_{CC(A)}$ or GND; for H1, H2, V1, V2: I_O = 0 A; SCLn, SDAn unconnected	-	-	2.0	µA
HV buffer						
V_{IH}	HIGH-level input voltage	$V_{CC(A)}$ = 3 V to 3.6 V	2	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC(A)}$ = 3 V to 3.6 V	-	-	0.8	V
V_H	hysteresis voltage		-	50	-	mV
I_I	input leakage current	$V_{CC(B)}$ = $V_{CC(A)}$ = 5.5 V; V_I = GND to $V_{CC(A)}$	-	-	±1	µA
V_{OH}	HIGH-level output voltage	I_O = −8 mA	$V_{CC(B)}$ − 0.5	-	-	V
V_{OL}	LOW-level output voltage	I_O = 8 mA	-	-	0.5	V
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 5.5 V; $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 0 V to 5.5 V	-	-	±1	µA
RGB switches						
$I_{S(OFF)}$	OFF-state leakage current	$V_{CC(B)}$ = 5.5 V; V_I = 0.3 V or 5.5 V; V_O = 0 V to $V_{CC(B)}$; EN = $V_{CC(A)}$ or GND; See Figure 3	-	-	±1	µA
$I_{S(ON)}$	ON-state leakage current	$V_{CC(B)}$ = 5.5 V; V_I = 0.3 V or 5.5 V; V_O = 0 V to $V_{CC(B)}$; EN = $V_{CC(A)}$; See Figure 4	-	-	±1	µA
R_{ON}	ON resistance	V_I = 0.7 V; I_{SW} = −10 mA; See Figure 5 and Figure 6 [4]	-	4	-	Ω

Table 8. Static characteristics *...continued*

$V_{CC(B)}$ = 4.5 V to 5.5 V; $V_{CC(A)}$ = 2 V to 5.5 V, unless otherwise specified; Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions		T_{amb} = −40 °C to +85 °C			Unit
				Min	Typ[1]	Max	
ΔR_{ON}	ON resistance mismatch between channels	V_I = GND to 0.7 V; I_{SW} = −10 mA	[2]	-	0.5	-	Ω
$R_{ON(flat)}$	ON resistance (flatness)	V_I = GND to 0.7 V; I_{SW} = −10 mA	[3]	-	0.5	-	Ω
$C_{S(OFF)}$	OFF-state capacitance			-	4.5	-	pF
$C_{S(ON)}$	ON-state capacitance			-	12	-	pF
SDAn, SCLn							
$I_{S(OFF)}$	OFF-state leakage current	$V_{CC(B)}$ = 5.5 V; $V_{CC(A)}$ = 3.6 V; SCL0, SDA0, SCL1, SCL2, SDA1, SDA2 = $V_{CC(A)}$ or GND; V_O = 0 V to $V_{CC(B)}$; EN = GND; See Figure 3	[5]	-	-	±1	μA
R_{ON}	ON resistance	$V_{CC(A)}$ = 2 V; V_I = 0.4 V; I_{SW} = ±2 mA; See Figure 5 and Figure 7		-	9	-	Ω
$C_{S(ON)}$	ON-state capacitance			-	15	-	pF
R_{PU}	pull-up resistance			-	4.7	-	kΩ
Control Logic (SEL, EN)							
V_{IH}	HIGH-level input voltage	$V_{CC(A)}$ = 2.3 V to 2.7 V		1.7	-		V
		$V_{CC(A)}$ = 3.0 V to 3.6 V		2.0	-		V
		$V_{CC(A)}$ = 4.5 V to 5.5 V		$0.7V_{CC(A)}$	-		V
V_{IL}	LOW-level input voltage	$V_{CC(A)}$ = 2.3 V to 2.7 V		-	-	0.7	V
		$V_{CC(A)}$ = 3.0 V to 3.6 V		-	-	0.8	V
		$V_{CC(A)}$ = 4.5 V to 5.5 V		-	-	$0.3V_{CC(A)}$	V
V_H	hysteresis voltage			-	50	-	mV
I_I	input leakage current	$V_{CC(A)}$ = 5.5 V; V_I = GND to $V_{CC(A)}$		-	-	±1	μA

[1] All typical values are measured at $V_{CC(B)}$ = 5 V, $V_{CC(A)}$ = 3.3 V and T_{amb} = 25 °C unless otherwise specified.

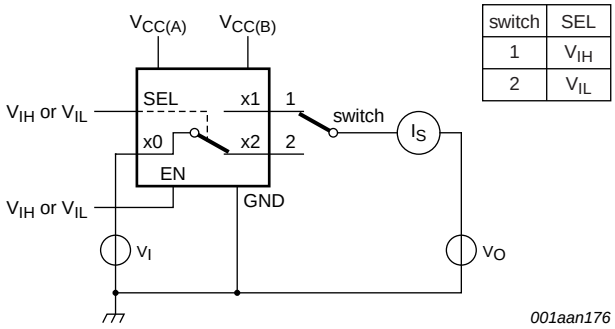
[2] Measured at identical V_{CC}, temperature and input voltage.

[3] Flatness is defined as the difference between the maximum and minimum value of ON resistance measured at identical V_{CC} and temperature.

[4] Guarantees the LOW level.

[5] Guarantees the HIGH level.

10.1 Test circuits and waveforms



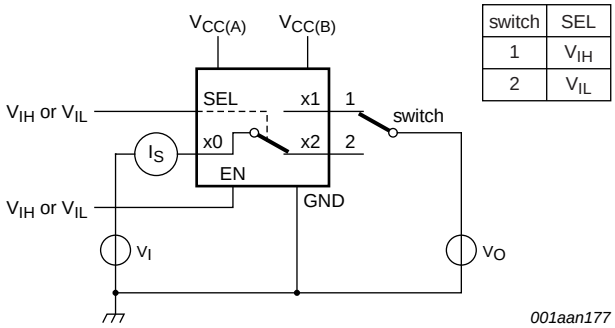
switch	SEL
1	V_{IH}
2	V_{IL}

x0 refers to R0, G0, B0, SCL0 or SDA0

x1 refers to R1, G1, B1, SCL1 or SDA1

x2 refers to R2, G2, B2, SCL2 or SDA2

Fig 3. Test circuit for measuring OFF-state leakage current



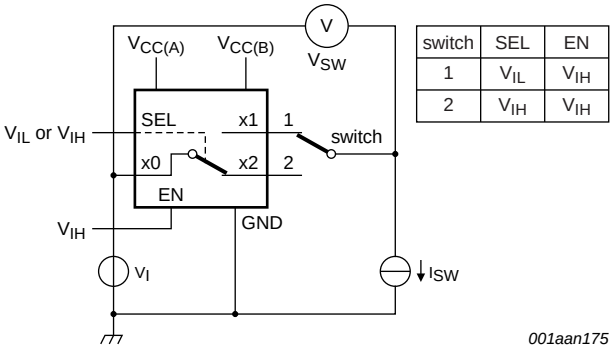
switch	SEL
1	V_{IH}
2	V_{IL}

x0 refers to R0, G0, B0, SCL0 or SDA0

x1 refers to R1, G1, B1, SCL1 or SDA1

x2 refers to R2, G2, B2, SCL2 or SDA2

Fig 4. Test circuit for measuring ON-state leakage current



switch	SEL	EN
1	V_{IL}	V_{IH}
2	V_{IH}	V_{IH}

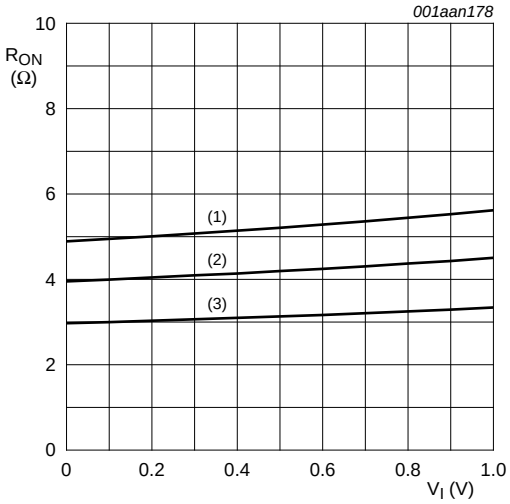
x0 refers to R0, G0, B0, SCL0 or SDA0

x1 refers to R1, G1, B1, SCL1 or SDA1

x2 refers to R2, G2, B2, SCL2 or SDA2

$R_{ON} = V_{SW} / I_{SW}$.

Fig 5. Test circuit for measuring ON resistance

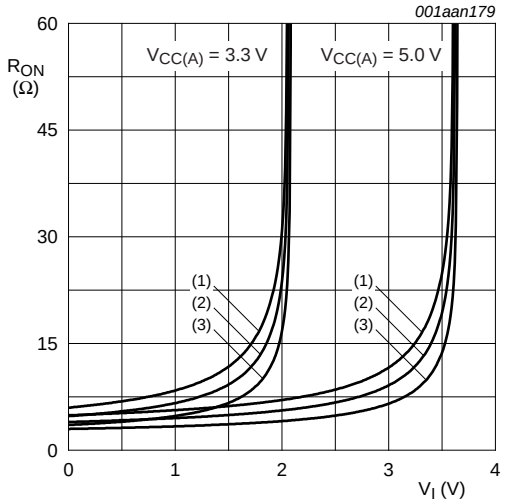


(1) T_{amb} = 85 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 6. ON resistance as a function of input voltage (RGB switches)



(1) T_{amb} = 85 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 7. ON resistance as a function of input voltage (DDC switches)

11. Dynamic characteristics

Table 9. Dynamic characteristics

At recommended operating conditions; Voltages are referenced to GND (ground = 0 V; $V_{CC(B)}$ = 4.5 V to 5.5 V; $V_{CC(A)}$ = 2 V to 5.5 V.

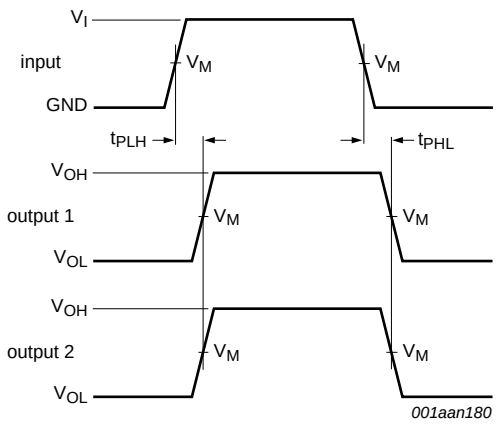
Symbol	Parameter	Conditions		T_{amb} = −40 °C to +85 °C			Unit
				Min	Typ[1]	Max	
t_{pd}	propagation delay	H0 to H1, H2 and V0 to V1, V2; See Figure 8 and Figure 9	[2]	-	3	-	ns
t_{en}	enable time	EN and SEL to all other outputs; See Figure 10 and Figure 11		-	15	-	ns
t_{dis}	disable time	EN and SEL to all other outputs; See Figure 10 and Figure 11		-	5	-	ns
t_{b-m}	break-before-make time	See Figure 12		-	10	-	ns
$t_{sk(o)}$	output skew time	Skew between any Rn, Gn and Bn ports; see Figure 8	[3]	-	50	-	ps

[1] All typical values are measured at $V_{CC(B)}$ = 5 V; $V_{CC(A)}$ = 3.3 V; T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] Guaranteed by design.

11.1 Test circuits and waveforms



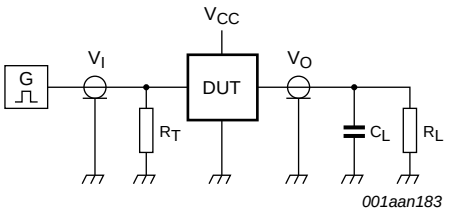
Measurement points are given in Table 10.

$t_{sk(o)} = |t_{PLH1} - t_{PLH2}|$

Fig 8. Test circuit for measuring propagation delay times

Table 10. Measurement points

Input		Output	
V_M	V_I	V_X	V_M
$0.5V_{CC(A)}$	GND to $V_{CC(A)}$	$0.9V_{OH}$	$0.5V_{CC(B)}$



Test data is given in Table 11.

Definitions:

DUT = Device Under Test.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

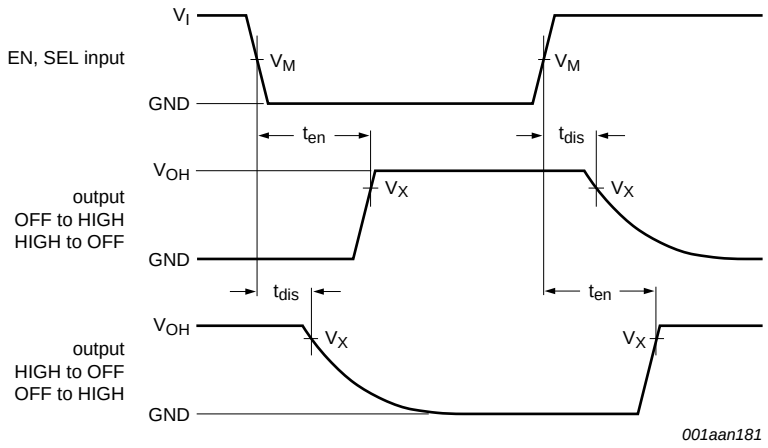
C_L = Load capacitance including test jig and probe.

R_L = Load resistance.

Fig 9. Test circuit for measuring propagation delay times

Table 11. Test data

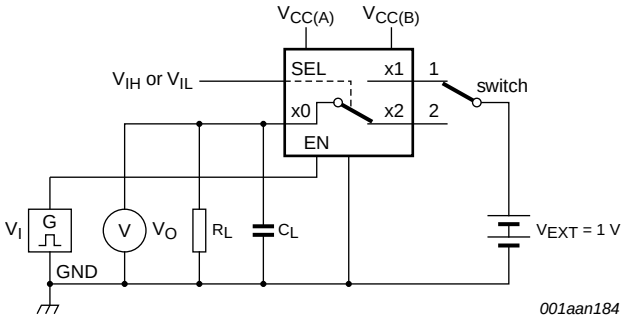
Input	Load	
t_r, t_f	C_L	R_L
≤ 2.5 ns	10 pF	1 kΩ



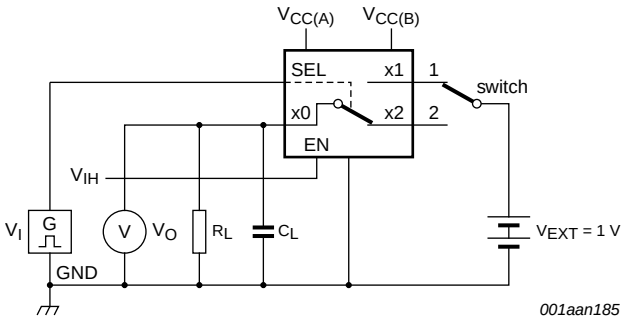
Measurement points are given in Table 10.

Logic level: V_{OH} is typical output voltage level that occurs with the output load.

Fig 10. Enable and disable times



a. EN to switch outputs



b. SEL to switch outputs

Test data is given in Table 12.

x0 refers to R0, G0, B0, SCL0 or SDA0

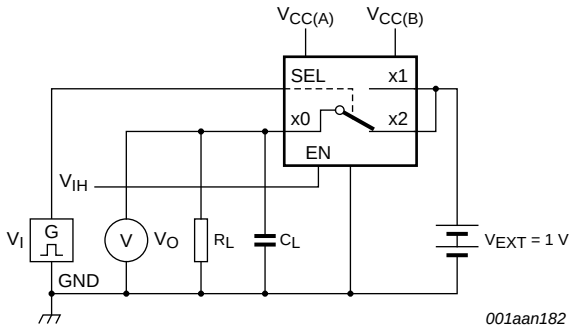
x1 refers to R1, G1, B1, SCL1 or SDA1

x2 refers to R2, G2, B2, SCL2 or SDA2

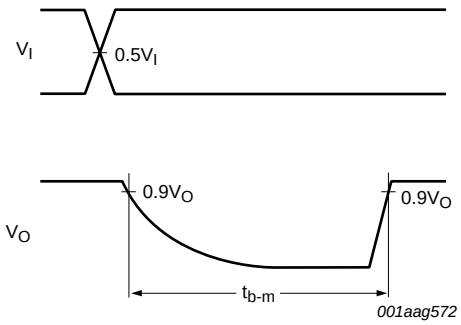
Fig 11. Test circuit for measuring enable and disable times

Table 12. Test data

Input		Load	
t_r, t_f	V_I	C_L	R_L
≤ 2.5 ns	GND to $V_{CC(A)}$	10 pF	100 Ω



a. Test circuit



b. Input and output measurement points

Test data is given in Table 12.

x0 refers to R0, G0, B0, SCL0 or SDA0

x1 refers to R1, G1, B1, SCL1 or SDA1

x2 refers to R2, G2, B2, SCL2 or SDA2

Fig 12. Test circuit for measuring break-before-make timing

12. Additional dynamic characteristics

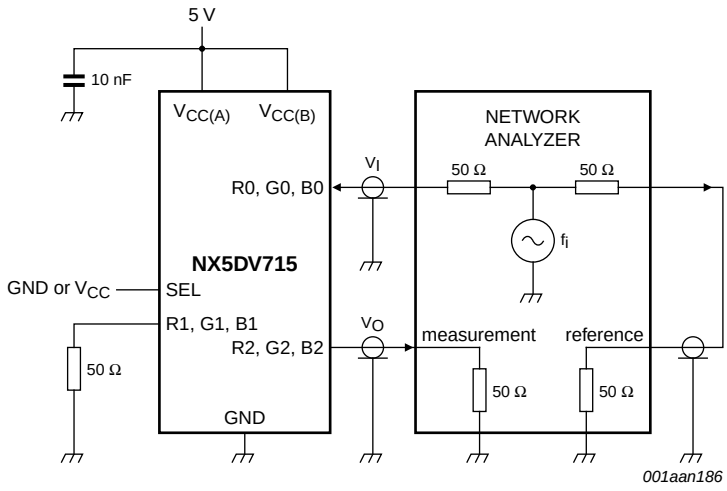
Table 13. Additional dynamic characteristics

$V_{CC(B)}$ = 5.0 V ± 10 %, $V_{CC(A)}$ = 2 V to 5.5 V, unless otherwise specified; Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions		T_{amb} = −40 °C to +85 °C			Unit
				Min	Typ	Max	
$f_{(-3dB)}$	−3 dB frequency response	R_L = 50 Ω; see Figure 13	[1]	-	600	-	MHz
α_{ins}	Insertion loss	f_i = 1 MHz; R_L = R_S = 50 Ω; see Figure 13		-	0.6	-	dB
Xtalk	crosstalk	between switches; f_i = 50 MHz; R_L = 50 Ω; see Figure 13	[1]	-	−50	-	dB

[1] f_i is biased at $0.5V_{CC}$.

12.1 Test circuits



Insertion loss is measured between R0 and R1 or R2 on each switch; crosstalk is measured from one channel to the other channel.

Fig 13. Test circuit for measuring crosstalk and insertion loss

13. Application information

The NX5DV715 provides the level shifting necessary to drive two standard VGA ports from a graphic controller as low as 2.2 V. Internal buffers drive the H-Sync and V-Sync signals to VGA standard TTL levels. The DDC multiplexer provides level shifting by clamping signals to a diode drop less than $V_{CC(A)}$ (See Figure 14). Connect $V_{CC(A)}$ to 3.3 V for normal operation, or to $V_{CC(B)}$ to disable voltage clamping for DDC signals

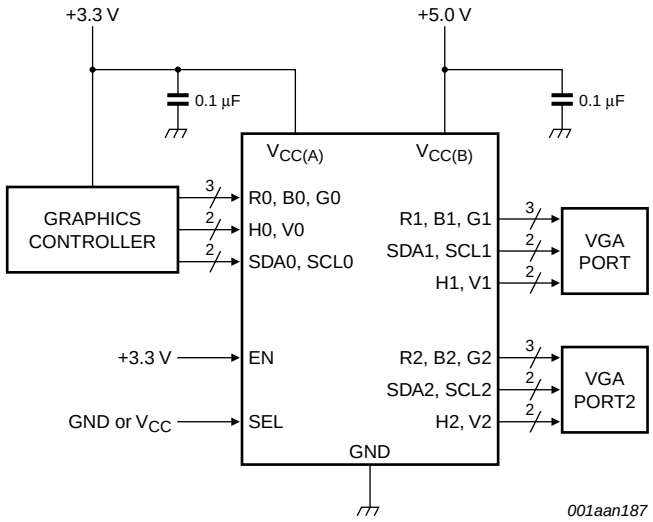
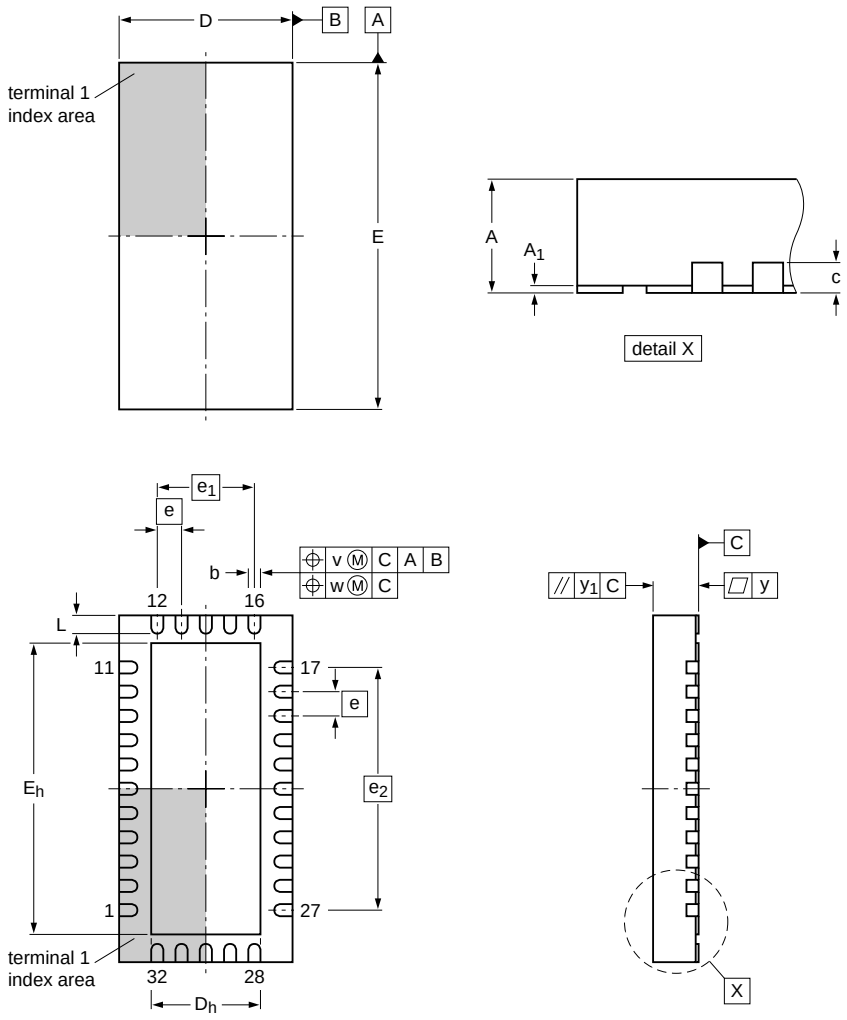


Fig 14. Typical operating circuit

14. Package outline

HWQFN32: plastic thermal enhanced very very thin quad flat package; no leads; 32 terminals; 3 x 6 x 0.75 mm **SOT1180-1**



Dimensions

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
	max	0.80	0.05	0.25		3.1	1.9	6.1	4.9				0.4				
mm	nom	0.75	0.02	0.20	0.2	3.0	1.8	6.0	4.8	0.4	1.6	4	0.3	0.07	0.05	0.08	0.1
	min	0.70	0.00	0.15		2.9	1.7	5.9	4.7				0.2				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1180-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1180-1	- - -	- - -	- - -			~~10-07-02~~ 10-08-05

Fig 15. Package outline SOT1180-1 (HWQFN32)

15. Abbreviations

Table 14. Abbreviations

Acronym	Description
CDM	Charged Device Model
DDC	Display Data Channel
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
RGB	Red Green Blue
TTL	Transistor-Transistor Logic
VESA	Video Electronics Standards Association

16. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX5DV715 v.3	20111104	Product data sheet	-	NX5DV715 v.2
Modifications:	• Legal pages updated			
NX5DV715 v.2	20110725	Product data sheet	-	NX5DV715 v.1
NX5DV715 v.1	20101220	Product data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

17.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

17.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

17.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

18. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

19. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 4 November 2011
Document identifier: NX5DV715