PSG5220

DATA SHEET

Dual-Channel Advanced Power Management IC with On-Demand Power®

1 Features

- Configurable On-Demand Power® algorithm to adaptively scale regulated output voltage in correlation with monitored system activity
- System sensory interfaces to monitor activity and demand for sub-domains on both regulated voltage domains
- Dual, constant-on-time, voltage feed-forward, synchronous step-down PWM controllers
- Wide input voltage range: 6.5V to 24V
- Programmable output voltage range: 3V to 5V
- PWM and light-load operation
- Temperature compensated $R_{DS(ON)}$ current sensing
- Internal softstart
- Output over and under voltage protection
- Built-in output discharge circuit
- SMBUS Interface
- 8x8mm or 7x7mm 56-pin QFN package

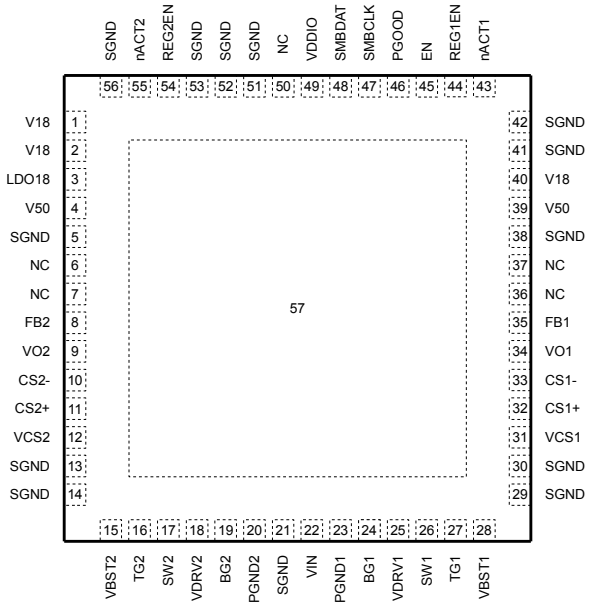
2 Description

The PSG5220 is a highly integrated power management IC with dual synchronous step-down PWM controllers for SATA drive power management in mobile computers as well as power management in embedded system applications. Interfaces for monitoring activity, coupled with advanced On-Demand Power algorithms, enable the regulated output voltages of the integrated switching regulators to be adaptively scaled in correlation with actual power demand. The real-time tracking of supply voltage to activity enables maximum power savings by minimizing the power spent on maintaining worst-case headroom in power distribution.

3 Applications

- Mobile Computers
- Ultra-Mobile PCs
- Portable Media Players
- Other Mobile Devices
- SATA drives

4 Pin Configuration



56-LEAD (8mm x 8mm) PLASTIC QFN
EXPOSED PAD (PIN 57) IS SGND. MUST BE SOLDERED TO PCB.

5 Absolute Maximum Ratings (Note 1)

PARAMETER	VALUE	UNIT
V50 to SGND	-0.3 to 6	V
VDRV1 to PGND1 and VDRV2 to PGND2	-0.3 to 6	V
V18 to SGND	-0.3 to 2.0	V
VDDIO to SGND	-0.3 to 6.0	V
VIN to SGND	-0.3 to 30	V
LDO18 to SGND	-0.3 to 2.0	V
VCS1 and VCS2 to SGND	-0.3 to 6	V
VO1, CS1+, and CS1- to VCS1	0.3	V
VO2, CS2+, and CS2- to VCS2	0.3	V
VO1, CS1+, and CS1- to SGND	-0.3 to 6	V
VO2, CS2+, and CS2- to SGND	-0.3 to 6	V
FB1 and FB2 to SGND	-0.3 to 2.0	V
VBST1 to PGND1 and VBST2 to PGND2	-0.3 to 30	V
VBST1 to SW1 and VBST2 to SW2	-0.3 to 6	V
SW1 to PGND1 and SW2 to PGND2	-2 to 30	V
BG1 to PGND1 and PG2 to PGND2	-0.3 to 6	V
BG1 to VDRV1 and BG2 to VDRV2	0.3	V
TG1 to PGND1 and TG2 to PGND2	-2 to 30	V
TG1 to SW1 and TG2 to SW2	-0.3 to 6	V
TG1 to VBST1 and TG2 to VBST2	0.3	V
All other pins to SGND	-0.3 to 6.0	V
All other pins to VDDIO	0.3	V
Maximum Junction Temperature	125	°C

Note 1 Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

6 Electrical Characteristics

Unless otherwise noted: V_{VIN} = 15V, V_{V50} = V_{VDRV} = V_{VDDIO} = 5V, V_{V18} = 1.8V, V_{SGND} = V_{PGND} = 0V, V_{EN} = V_{REG1EN} = V_{REG2EN} = 5V, V_{SMBDAT} = V_{SMBCLK} = 5V, V_{nACT1} = V_{nACT2} = 5V, V_{PGOOD} = 5V, LDO18 = No Load, T_A = 0°C to 70°C. Typical values are at T_A = 25°C.

Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage		6.5		24	V
V_{V18}	Digital and analog supply voltage		1.62	1.8	1.98	V
V_{VDDIO}	Digital IO supply voltage		4.5	5	5.5	V
V_{V50}	Analog supply voltage		4.5	5	5.5	V
V_{VDRV}	Bottom gate drive supply voltage		4.5	5	5.5	V
V_{TGDRV}	Top gate drive supply voltage	V_{TGDRV} = V_{VBST} - V_{SW}	4.5	5	5.5	V
V_{VCS}	Differential amplifier supply voltage		4.0	5	5.5	V
T_J	Operating junction temperature		0		70	°C

Power Supplies

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{V18}	Digital and analog supply current Enabled Disabled	 $V_{EN} = V_{REG1EN} = V_{REG2EN} = 5V$ $V_{EN} = V_{REG1EN} = V_{REG2EN} = 0V$			 2.1 30	 mA µA
I_{VDDIO}	Digital IO supply current	No switching outputs			25	µA
I_{V50}	Analog supply current Enabled Disabled	No load on LDO18 output $V_{EN} = V_{REG1EN} = V_{REG2EN} = 5V$ $V_{EN} = V_{REG1EN} = V_{REG2EN} = 0V$			 3 80	 mA µA
I_{VDRV}	Bottom gate driver supply current Enabled Disabled	Per channel. All gate drivers are output low $V_{EN} = V_{REG1EN} = V_{REG2EN} = 5V$ $V_{EN} = V_{REG1EN} = V_{REG2EN} = 0V$			 250 34	 µA µA
I_{VBST}	Top gate driver supply current Enabled Disabled	Per channel. All gate drivers are output low. $V_{EN} = V_{REG1EN} = V_{REG2EN} = 5V$ $V_{EN} = V_{REG1EN} = V_{REG2EN} = 0V$			 300 150	 µA µA
I_{VCS}	Differential amplifier supply current Enabled	Per channel. $V_{EN} = V_{REG1EN} = V_{REG2EN} = 5V$, $V_{VCSx} = V_{CSx+} = V_{CSx-} = 5V$			80	µA

Digital Interface

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
SMBDAT, SMBCLK Inputs						
V_{IH}	Input high voltage				2.1	V
V_{IL}	Input low voltage		0.8			V
$I_{IN(1)}$	Input current for input high voltage	Input Voltage = 5V (Note 2)			-5	µA
$I_{IN(0)}$	Input current for input low voltage	Input Voltage = 0V (Note 2)			5	µA
nACT1, nACT2 Inputs						
V_{IH}	Input high voltage				1.4	V
V_{IL}	Input low voltage		0.8			V
$I_{IN(1)}$	Input current for input high voltage	Input Voltage = 5V			-10	µA
$I_{IN(0)}$	Input current for input low voltage	Input Voltage = 0V			10	µA
EN, REG1EN, REG2EN Inputs						
V_{IH}	Input high voltage				2.1	V
V_{IL}	Input low voltage		0.8			V
$I_{IN(1)}$	Input current for input high voltage	Input Voltage = 5V			-10	µA
$I_{IN(0)}$	Input current for input low voltage	Input Voltage = 0V			10	µA
SMBDAT Output						
V_{OL}	Low level output voltage	I_{OL} = 2mA			0.4	V
I_{OH}	High level output leakage current	Output Voltage = 5V (Note 2)			5	µA
PGOOD Output						
V_{OL}	Low level output voltage	I_{OL} = 2mA			0.4	V
I_{OH}	High level output leakage current	Output Voltage = 5V			10	µA

SMBus Interface (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{SMB}	SMBus clock frequency		10		100	kHz
t_{LOW}	SMBus clock low time	Measured from $V_{IL(MAX)}$ to $V_{IL(MAX)}$	4.7			µs
t_{HIGH}	SMBus clock high time	Measure from $V_{IH(MIN)}$ to $V_{IH(MIN)}$	4.0			µs
$t_{r,SMB}$	SMBus rise time	(Note 4)			1	µs
$t_{f,SMB}$	SMBus fall time	(Note 5)			0.3	µs
t_{OF}	Output fall time	C_L = 400 pF, I_O = 3mA, (Note 5)			250	ns
$t_{TIMEOUT}$	SMBDAT and SMBCLK time low for reset of SMBus	(Note 6)	25		35	ms

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$t_{SU,DAT}$	Data setup time		250			ns
$t_{HD,DAT}$	Data hold time		300			ns
$t_{HD,STA}$	Hold time after (repeated) start condition. After this period, the first clock is generated.		4			µs
$t_{SU,STO}$	Stop condition setup time		4			µs
$t_{SU,STA}$	Repeated start condition setup time		4.7			µs
t_{BUF}	Bus free time between stop and start conditions		4.7			µs

5MHz Internal Oscillator

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{5MHZ}	Internal oscillator frequency		4.5		5.5	MHz

Switching Regulators

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Gate Drivers						
$R_{TG(UP)}$	TG driver pull-up on resistance	TG high		2.1	8	Ω
$R_{TG(DOWN)}$	TG driver pull-down on resistance	TG low		1.5	4	Ω
$R_{BG(UP)}$	BG driver pull-up on resistance	BG high		1.4	8	Ω
$R_{BG(DOWN)}$	BG driver pull-down on resistance	BG low		0.7	4	Ω
$t_{DEAD(TG/BG)}$	Dead time	TG low to BG high (Note 7)		53		ns
$t_{DEAD(BG/TG}$	Dead time	BG low to TG high (Note 7)		30		ns
V_{OUT} Discharge						
I_{DISCHG}	V_{OUT} discharge current	V_{EN} = 5V, V_{REGxEN} = 0V, V_{VOx} = 0.5V	10			mA
Duty and Frequency Control						
$t_{ON(1)}$	On time	V_{VIN} = 24V, VSETx[7:0] = 00h		335		ns
$t_{ON(2)}$	On time	V_{VIN} = 21V, VSETx[7:0] = 00h		391		ns
$t_{ON(3)}$	On time	V_{VIN} = 19V, VSETx[7:0] = 00h		436		ns
$t_{ON(4)}$	On time	V_{VIN} = 17V, VSETx[7:0] = 00h		508		ns
$t_{ON(5)}$	On time	V_{VIN} = 15.5V, VSETx[7:0] = 00h		569		ns
$t_{ON(6)}$	On time	V_{VIN} = 12V, VSETx[7:0] = 00h		824		ns
$t_{ON(7)}$	On time	V_{VIN} = 11.6V, VSETx[7:0] = 00h		863		ns
$t_{ON(8)}$	On time	V_{VIN} = 9.9V, VSETx[7:0] = 00h		1.160		µs
$t_{ON(9)}$	On time	V_{VIN} = 8.5V, VSETx[7:0] = 00h		1.604		µs
$t_{ON(10)}$	On time	V_{VIN} = 7.5V, VSETx[7:0] = 00h		2.222		µs
$t_{OFF(MIN)}$	Minimum off time			300		ns
$t_{DEAD(MAX)}$	DCM timeout			1026	1130	ns
Softstart						
$t_{SS(10)}$	Softstart time		1.2		2.5	ms
Powergood (PG)						
$V_{PG(L)}$ $V_{PG(H)}$	PG trip voltage Lower PG trip voltage Upper PG trip voltage	With respect to set regulated voltage V_{VOx} = 4V to 5V V_{VOx} ramping negative V_{VOx} ramping positive	 -600 300		 -300 600	 mV mV
t_{PGDEL}	PG delay	Entering PG window	115	130	145	µs
Over Voltage Protection (OVP)						
$V_{OVP(F)}$	Fixed OVP trip voltage		5.6		5.9	V
$V_{OVP(D)}$	Dynamic OVP trip voltage	With respect to set regulated voltage V_{VOx} = 4V to 5V	0.8		1.4	V
t_{OVPDEL}	OVP prop delay			10		µs

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Under Voltage Protection (UVP)						
V_{UVP}	UVP trip voltage		1.08		1.32	V
t_{UVPDEL}	UVP prop delay		25		40	µs
t_{UVPEN}	UVP enable delay	From rising edge of REGxEN	1.9		3.8	ms
Current Sense						
$V_{OCP(OFF)(6)}$	Over current protection offset voltage	OCPROGx[3:0]=6h		35		mV
$TC_{OCP(6)}$	Over current protection temperature coefficient	OCPROGx[3:0]=6h		131		µV/°C
$V_{OCP(OFF)(8)}$	Over current protection offset voltage	OCPROGx[3:0]=8h		45		mV
$TC_{OCP(8)}$	Over current protection temperature coefficient	OCPROGx[3:0]=8h		168		µV/°C
$V_{OCP(OFF)(A)}$	Over current protection offset voltage	OCPROGx[3:0]=Ah		55		mV
$TC_{OCP(A)}$	Over current protection temperature coefficient	OCPROGx[3:0]=Ah		205		µV/°C
$V_{OCP(OFF)(C)}$	Over current protection offset voltage	OCPROGx[3:0]=Ch		65		mV
$TC_{OCP(C)}$	Over current protection temperature coefficient	OCPROGx[3:0]=Ch		243		µV/°C
V_{ZC}	Zero cross detection comparator offset		-5		8	mV
Programmable Output Voltage						
$V_{PROG(MAX)}$	Maximum programmable output voltage		4.8			V
$V_{PROG(MIN)}$	Minimum programmable output voltage				4	V
$V_{PROG(ERROR)}$	Programmable output voltage error	VSETx[7:0] = 00h to 55h, V50 = 4.5V to 5.5V, V18 = 1.62V to 1.98V		14.95	120	mV

1.8V Linear Regulator

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{LDO18}	1.8V LDO output voltage	$0 < I_{LDO18} < 5mA$	1.71		1.98	V

Current Sense

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
t_p	Propagation delay	$V_{CSx+} - V_{CSx-}$ = 10mV to 90mV, ITRIP = 50mV, V_{VCSx} = 5V			10	µs
I_{CS+}	CS1+ and CS2+ input bias current	V_{VCSx} = 5V, V_{CSx+} = 5V, V_{CSx-} = 4V to 5V			120	nA
I_{CS-}	CS1+ and CS2+ input bias current	V_{VCSx} = 5V, V_{CSx+} = 5V, V_{CSx-} = 4V to 5V			10	µA
$V_{TRIP(90)}$	Programmable trip voltage	ISETx[7:0] = C6h		90		mV
$V_{TRIP(10)}$	Programmable trip voltage	ISETx[7:0] = 10h		10		mV

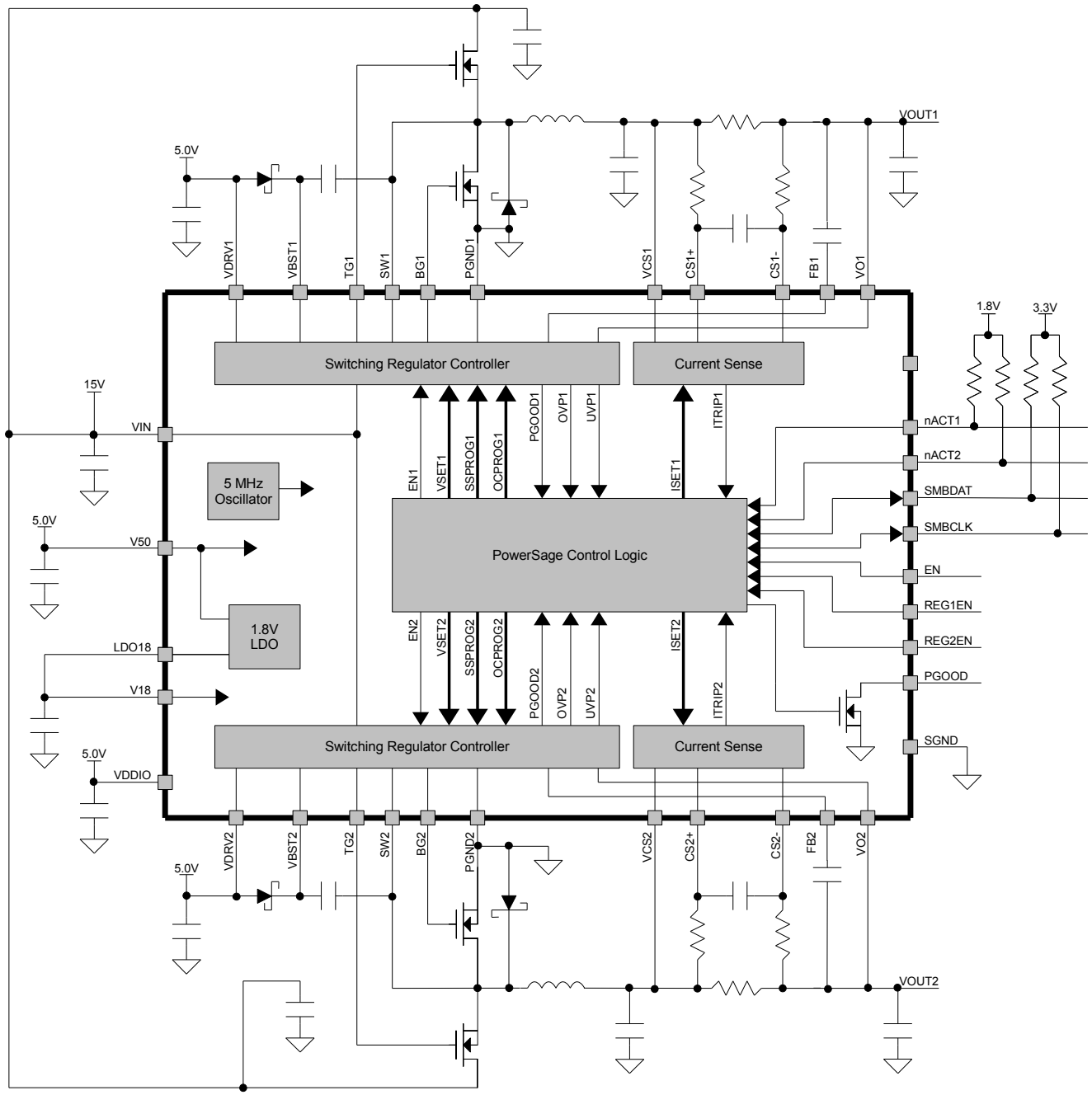
Note 2 Parts are tested at 25°C. Temperature limits established by characterization and are not production tested.
Note 3 Unless otherwise noted, these specifications apply for load capacitances on SMBus lines = 80pF. The switching characteristics of the PSG5220 fully meet or exceed the published specifications of the SMBus version 2.0.
Note 4 The rise time is measured from ($V_{IL(MAX)}$ - 0.15V) to ($V_{IH(MIN)}$ + 0.15V).
Note 5 The fall time is measured from ($V_{IH(MIN)}$ + 0.15V) to ($V_{IL(MAX)}$ – 0.15V).
Note 6 Exceeding $t_{TIMEOUT}$ will reset the PSG5220 SMBus state machine, therefore setting SMBDAT and SMBCLK pins to a high impedance state.
Note 7 Delay times are measured using 50% levels.
Note 8 Guaranteed by design.

7 Pin Functions

NAME	PIN	IO (Note 9)	DESCRIPTION
V18	1, 2, 40	P	1.8V power supply for both digital and analog circuitry. Decouple each pin to SGND with a capacitor.
VDDIO	49	P	IO power supply. Decouple to SGND with a capacitor. This is the input supply for digital IO drivers and receivers.
V50	4, 39	P	5V power supply for analog circuitry. Decouple each pin to SGND with a capacitor.
VIN	22	P	High voltage sense input. Decouple to SGND with a capacitor.
SGND	5, 13-14, 21, 29-30, 38, 41, 42, 51, 52, 53, 56, 57	P	Small signal ground. All small signal components should connect to this ground. Connect SGND to PGND1,2 at one point. Pin 57 is the exposed pad.
PGND1,2	20, 23	P	Channel 1 and 2 power grounds. Connect these closely to the appropriate sources of the bottom external N-channel MOSFETs and the negative terminal of the VDRV1,2 decoupling capacitors. Connect PGND1,2 to SGND at one point.
VDRV1,2	25, 18	P	Channel 1 and 2 bottom gate driver supply. Decouple to its respective PGND with a capacitor.
LDO18	3	PO	Internal 1.8V linear regulator output. Decouple to SGND with a capacitor. This output can be connected to V18 as the 1.8V supply.
VCS1,2	31, 12	P	Channel 1 and 2 differential amplifier supply voltage. Typically connected to the load side of its respective power inductor. Decouple to SGND with a capacitor.
CS1,2+	32, 11	A	Channel 1 and 2 current sense differential amplifier inputs. The positive inputs to the amplifiers are normally connected to current sensing resistors through an RC filter.
CS1,2-	33, 10	A	Channel 1 and 2 current sense differential amplifier inputs. The negative inputs to the amplifiers are normally connected to current sensing resistors through an RC filter.
VO1,2	34, 9	A	Channel 1 and 2 output voltage remote sense inputs.
FB1,2	35, 8	A	Channel 1 and 2 output voltage feedback. Connection point for external ripple injection circuitry or leave floating.
nACT1,2	43, 55	I	Channel 1 and 2 activity inputs. A logic low indicates that the respective load is active. A logic high indicates that the respective load is idle. Connect directly to VDDIO if not used. Do not leave floating.
SMBDAT	48	IOD	SMBus data input/output. The PSG5220 is configured as an SMBus device.
SMBCLK	47	IOD	SMBus clock input. The PSG5220 is configured as an SMBus device.
PGOOD	46	OD	Power good indicator output. This open-drain output is pulled to ground when either the channel 1 or channel 2 regulated output voltages leave the regulation window. Each regulator has a fixed 512us power good delay. Each channel has an additional programmable delay and mask.
EN	45	I	Enable input. A logic low disables the switching regulators and forces the PSG5220 into a low-power standby mode. A logic high enables the PSG5220. Switching regulator operation is also dependent on the REG1EN and REG2EN inputs. Connect directly to VDDIO if not used. Do not leave this pin floating. The output discharge circuits are disabled when EN is a logic low.
REG1EN	44	I	Channel 1 regulator enable input. A logic low disables the channel 1 regulator and activates the output discharge circuit. When the input is a logic high, the operational state of the channel 1 regulator is dependent on the internal channel 1 regulator enable bit. Connect directly to VDDIO if not used. Do not leave this pin floating.
REG2EN	54	I	Channel 2 regulator enable input. A logic low disables the channel 2 regulator and activates the output discharge circuit. When the input is a logic high, the operational state of the channel 2 regulator is dependent on the internal channel 2 regulator enable bit. Connect directly to VDDIO if not used. Do not leave this pin floating.
VBST1,2	28, 15	P	Boosted floating driver supplies for the channel 1 and 2 top gate drivers.
SW1,2	26, 17	A	Channel 1 and 2 switch node connections to power inductors.
TG1,2	27, 16	AO	Channel 1 and 2 top gate driver outputs.
BG1,2	24, 19	AO	Channel 1 and 2 bottom gate driver outputs.
NC	6, 7, 36, 37, 50	X	No Connect. These pins should be left floating.

Note 9 P = Power, A = Analog, I = Input, O = Output, OD = Open Drain, IOD = Bidirectional Open Drain, X = Unconnected

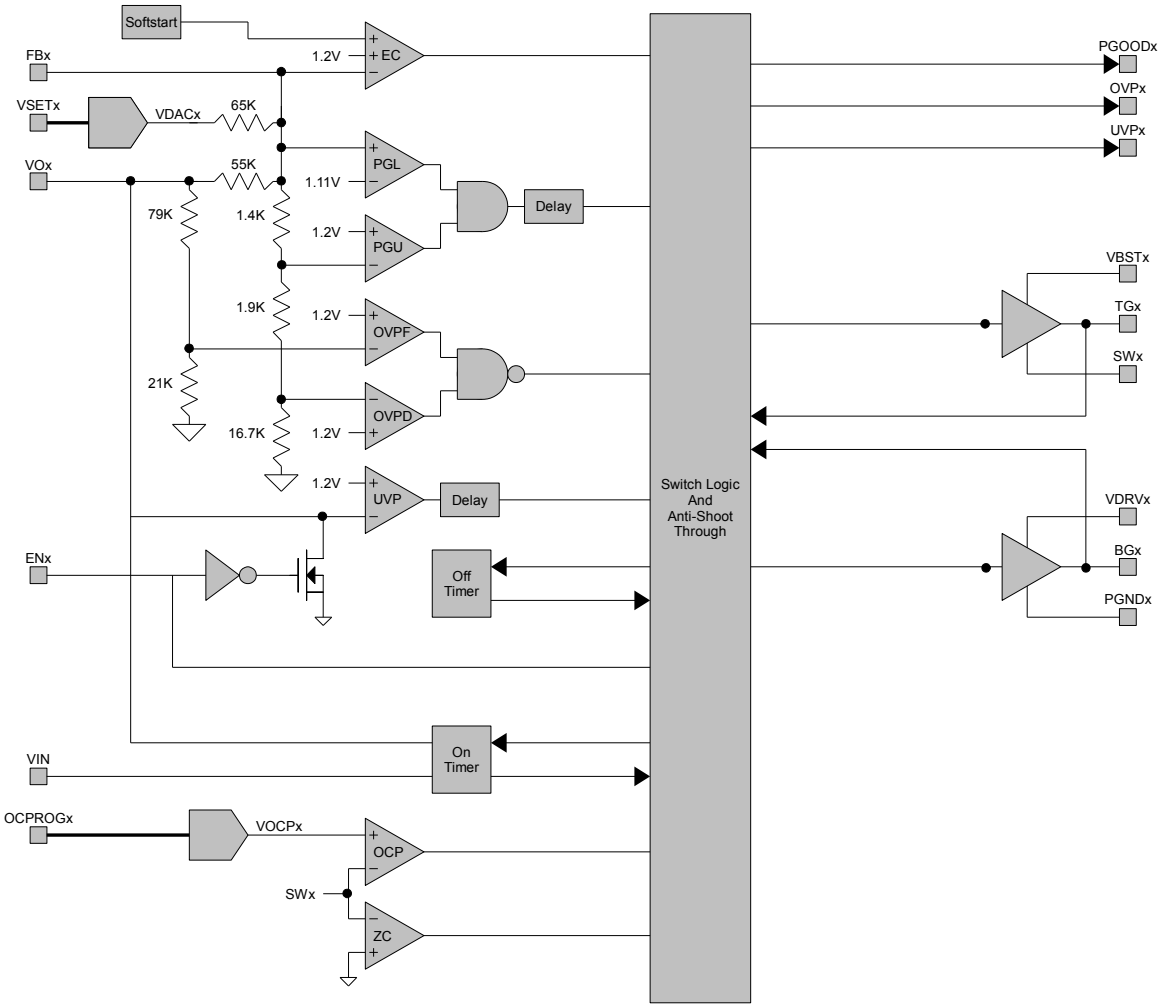
7.1 Functional Diagram



7.2 Synchronous PWM controller

This is a high efficiency constant on time input voltage feed-forward step-down synchronous PWM controller. The controller automatically switches between continuous conduction mode (CCM) and discontinuous conduction mode (DCM) depending on the average inductor current. In CCM, the top external MOSFET is turned on when the error comparator shows that the output voltage is in error. The top external MOSFET remains on for a fixed amount of time that is dependent on the input and output voltage relationship. When the top external MOSFET is turned off, the bottom external MOSFET is turned on until the inductor current is less than the valley current limit and the error comparator shows that output voltage is in error.

In DCM, the inductor current is not allowed to reverse. Therefore, the bottom MOSFET is turned off when the inductor current reaches zero. Both the top and bottom external MOSFETs remain off until the top external MOSFET is turned on when the error comparator shows that the output voltage is in error. During the time that both external MOSFETs are turned off, the output voltage is supplied by the output capacitor.



7.2.1 On-Time/Off-Time

The on-time of the PWM controller is dynamically adjusted on a cycle-by-cycle basis to maintain a constant ripple current in the power inductor. The input and output voltage of the switching regulator is monitored to adapt the period of a one-shot timer that sets the on-time of the controller. The typical on-time for channel 1 and channel 2 is:

$$t_{ONx} = \frac{5.83\mu V \cdot s}{V_{VIN} - V_{VOx}}$$

The off-time is dependent on the instantaneous voltage error and the minimum off time. For a constant load and constant input/output voltage, the off time for each channel can be estimated by:

$$t_{OFFx} \approx t_{ONx} \frac{(V_{VIN} - V_{VOx})}{V_{VOx}}$$

Since the on-time and off-time can be estimated for a constant load and constant input/output voltage, the switching frequency for each channel can be estimated in this condition by:

$$f_{SWx} \approx \frac{1}{t_{ONx} + t_{OFFx}}$$

7.2.2 DCM Operation

During light load, the PWM controller enters discontinuous conduction mode, DCM, to maintain high conversion efficiency. DCM is entered when the inductor valley current reaches zero and the bottom external MOSFET is turned off to prevent the inductor current from reversing. This decreases the effective switching frequency of the controller and reduces conversion losses in the MOSFET drivers. When both the top and bottom external MOSFETs are off, the output voltage is maintained by the output capacitance. Once the light load discharges the output capacitance to the point where the error comparator detects that the output voltage is in error, a new switching cycle is started by turning on the top external MOSFET. The on-time is not

effected. The load current where the controller transitions between CCM and DCM is:

$$I_{LOAD,trans} = \frac{1}{2}\left(\frac{V_{VIN} - V_{VOx}}{L_x}\right) t_{ONx}$$

The time both external MOSFETs can remain off is dependent on the instantaneous voltage error and the DCM timeout. For a constant load and constant input/output voltage, the DCM time for each channel can be estimated by:

$$t_{DCMx} \approx \frac{(t_{ONx} + t_{OFFx}) I_{LOAD,trans}}{I_{VOx}} - (t_{ONx} + t_{OFFx})$$

Since the on-time, off-time, and DCM time can be estimated for a constant load and constant input/output voltage, the switching frequency for each channel can be estimated in this condition by:

$$f_{SWx} \approx \frac{1}{t_{ONx} + t_{OFFx} + t_{DCMx}}$$

The maximum time both external MOSFETs can remain off while in DCM mode is limited to 1026µs. In the event of a DCM timeout, the bottom external MOSFET is turned on first for the minimum off-time to recharge the boost capacitor. Subsequently, the top external MOSFET is only turned on if the error comparator detects that the output voltage is in error.

7.2.3 External Ripple Injection

External ripple injection is used to couple extra output ripple to the error comparator through the VFBx pin. Correctly choosing this capacitor can minimize jitter in the switching frequency and allow for reduced output ripple. Internally there is a 20KOhm equivalent series resistance. The circuit should be designed to pass frequencies near and above 50kHz. If there will be noisy signals in close proximity to the PSG5220 a Band pass filter that passes frequencies between 50k and 5MHz will be optimal. A simple high pass filter can be designed on the following formula:

$$f = \frac{1}{2 \times \pi \times R \times C}$$

A 180pF series capacitor from VOUTx to VFBx is a reasonable circuit for the external ripple injection for most conditions.

7.2.4 MOSFET Drivers

Both the top and bottom MOSFET drivers are designed to drive N-channel external power MOSFETs. The bottom MOSFET driver pulls BGx down to PGNDx to turn off the external MOSFET, and it pulls BGx up to VDRVx to turn on the external MOSFET. Likewise, the top external MOSFETs driver pulls TGx down to SWx to turn off the external MOSFET, and it pulls TGx up to VBSTx to turn on the external MOSFET. The combined power dissipation of both MOSFET drivers in a single PWM controller channel attributed to switching events is:

$$P_{DISx} = V_{VDRVx} \times f_x \times (Q_{Tx} + Q_{Bx})$$

where f_x is the switching frequency, Q_{Tx} is the gate charge of the top external MOSFET, and Q_{Bx} is the gate charge of the bottom external MOSFET.

The top MOSFET driver has a floating power supply V_{VBSTx} - V_{SWx} that is derived from the 5V supply using a boost capacitor and boost diode. The boost capacitor is recharged through the boost diode from the 5V supply whenever the bottom external MOSFET is turned on and SWx is pulled to PGND.

7.2.5 Anti-Shoot Through Circuitry

In a synchronous PWM topology, it is possible to get shoot-through current from VIN to PGND when both the top and bottom external MOSFETs are fully or partially conducting. To prevent this, a dead time where both MOSFETs are off is internally generated by adding a delay from the turn off of the top external MOSFET to the turn on of the bottom external MOSFET and from the turn off of the bottom external MOSFET to the turn on of the top external MOSFET. The voltage and discharge current of both the top and bottom external MOSFETs are monitored to dynamically optimize the driver dead time and increase conversion efficiency.

7.2.6 Start-Up

The channel 1 PWM controller is enabled when both the EN and REG1EN pins are driven high. Likewise, the channel 2 PWM controller is enabled when both the EN and REG2EN pins are driven high. When enabled, there is a brief delay while the internal analog circuitry is powered-on and stabilized. Next, an internal DAC, one per channel, linearly ramps the error comparator reference voltage from 0V to VREF. This forces the regulated output voltage of the enabled channel to linearly increase from 0V to the final programmed output voltage in 1.5ms.

7.2.7 Shutdown

The channel 1 PWM controller is disabled when either the EN or REG1EN pins are driven low. Likewise, the channel 2 PWM controller is disabled when either the EN or REG2EN pins are driven low. When disabled, the internal analog circuitry of the PWM controller is forced into a low power mode. Also, the regulator output is discharged through it's respective VOx pin with a

internal limited current sink.

7.2.8 Output Discharge Circuitry

A 10mA minimum output discharge current sink is connected through VOx for each channel. The output discharge is active when the respective REGENx pins are driven low. The output discharge circuitry is not active when EN is driven low.

7.2.9 Powergood

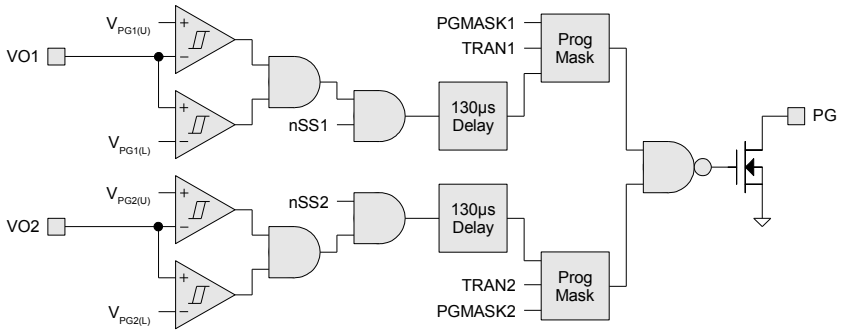
The PGOOD pin is an open-drain output that indicates if the output voltages of the PWM controllers, measured at pins VO1 and VO2, are within regulation. In fixed output voltage operation, the PGOOD pin is high impedance if both regulator outputs are within regulation, and the PGOOD pin is pulled to ground if either regulator output is out of regulation. Additionally, the PGOOD pin is pulled low if either channel is disabled or operating in soft-start. The power good regulation window is defined in the Electrical Characteristics table.

To minimize the effect of noise on the VO1 and VO2 pins, there is an internal fixed 130µs delay on the PGOOD output from both channels. Thus, VO1 or VO2 must be inside the regulation window for at least 130µs before the PGOOD pin becomes high impedance. However, the PGOOD pin will be pulled low immediately after VO1 and VO2 leave the regulation window.

During controlled output voltage transitions, a programmable masking of the PGOOD signal is enabled. While the On-Demand Power® controller is ramping either VSET control voltage from one fixed voltage to a new fixed voltage, the PGOOD pin will retain its state previous to the beginning of an output voltage transition until the output voltage is complete. Thus, if the PGOOD pin was pulled low at the beginning of a voltage transition, the PGOOD pin will remain pulled low throughout the entire output voltage transition, even if the transition event causes both output voltages to enter the regulation window. Likewise, if the PGOOD pin was high impedance at the beginning of a voltage transition, the PGOOD pin will remain high impedance throughout the entire output voltage transition, even if the transition event causes one of the output voltages to leave the regulation window. The programmable mask during output voltage transitions enable the On-Demand Power® controller to adjust the programmed output voltage VSET at a rate faster than the output of the PWM controllers can respond without inadvertently causing the PGOOD pin to be pulled low.

Furthermore, the programmable mask can be optionally extended for a programmable time period past the completion of an output voltage transition event. This feature allows the PWM controller output voltage some time to settle within the regulation window after a voltage transition occurs. This can be important when the output voltage step is large and/or the slew rate of VSET is high.

The complete powergood logic is shown below. nSS1 and nSS2 are low when the respective PWM controller is operating in softstart mode. TRAN1 and TRAN2 indicate if VSET for the respective switching regulator is transitioning. PGMASK1 and PGMASK2 set the programmable mask time period.



Powergood logic

7.2.10 Output Voltage Programming

The regulated output voltage of the PWM controllers is controlled with a DAC that is programmed by the On-Demand Power® controller.

$$V_{VOx} = 5 - \left[3\frac{VSETx[7:0]}{256}\right]$$

7.2.11 Over Current Protection

Over current protection is provided by monitoring the drain-to-source voltage across the bottom external MOSFET when it is turned on. As long as the sensed voltage drop is greater than the programmed voltage threshold, the bottom external MOSFET is forced to remain on. This effectively limits the maximum value of the power inductor valley current.

The channel 1 and 2 over current protection limits are independently programmed with the OCPROGx bits over the SMBus interface. The voltage threshold is temperature compensated to match the temperature dependency of the bottom external MOSFET. The programmed voltage threshold is:

$$V_{THx} = 0.37893(OCPROGx+1)((4.94\times10^{-5})T_J+0.01196)$$

For improved accuracy, there should be a good thermal connection between the MOSFET and the PSG5220.

7.2.12 Output Over and Under Voltage Protection

The output voltage of the PWM controllers is sensed at the VO1 and VO2 pins. If the sensed voltage exceeds either the fixed output over voltage threshold or the dynamic over voltage threshold, the bottom external MOSFET of the PWM controller experiencing the over voltage conditions is turned on to discharge the output capacitance and return the output voltage to safe operating level. Once the over voltage condition is no longer sensed, the PWM controller resumes normal operation.

When the sensed output voltage drops below the under voltage threshold, the PWM controller experiencing the under voltage condition is automatically disabled. The EN pin or REGxEN pin associated with the disabled PWM controller must be toggled to clear the under voltage condition. This response is desired because an under voltage condition will follow an output short circuit that triggers the over current protection circuitry. This protects the PWM controller and associated circuitry against an output short circuit.

7.2.13 UVLO Protection

All power supplies are monitored to ensure they are of suitable voltage before the PWM controllers are enabled.

7.3 Regulator Circuit Design

7.3.1 Inductor Selection

The maximum load current and inductor ripple current determine the value of the inductor. The value of the inductor ripple current ΔI_L can be calculated with input voltage V_{IN}, output voltage V_{Ox}, and on time t_{ONx}:

$$\Delta I_L = t_{ONx}\left(\frac{V_{VIN}-V_{VOx}}{L}\right)$$

Since the on-time of the PWM controller is adjusted to maintain a constant ripple current, ΔI_L is determined solely by the inductance value. A lower ripple current improves efficiency by reducing losses in the inductor and ESR losses in the input and output capacitors at the cost of a physically larger inductor. A ΔI_L that is 25% to 50% of $I_{LOAD(MAX)}$ is reasonable for balancing efficiency and inductor size.

An inductor should be selected to have the lowest possible DC resistance to maximize efficiency. Care must be taken to not saturate at the peak inductor current which can be determined by:

$$I_{L(PEAK)} = I_{LOAD(MAX)}+\frac{\Delta I_L}{2}$$

7.3.2 Output Capacitor Selection

Equivalent series resistance (ESR) is a dominant qualification for output capacitor selection. Specialty polymer capacitors, such as Sanyo POSCAP, are recommended due to high ripple current capability and low ESR at operation frequencies.

Output capacitance should be selected to provide an acceptable output voltage ripple ΔV_{VOx} which can be determined by the ESR and magnitude of the output capacitor. The capacitance must be sufficiently large for stability, however the capacitance value relates to the increasing physical size needed to decrease ESR. Consequently, the selection of C_{OUT} is primarily driven by ESR and can be found by:

$$ESR \leq \frac{\Delta V_{VOx}}{\Delta I_L}$$

7.3.3 Input Capacitor Selection

Select the input capacitors based on the expected maximum input ripple RMS current. This current varies with the load, input voltage, and phase of both PWM controllers. Since each channel operates at different frequencies, the worst-case phase causing an overlap in current pulses occurs over a short time duration. The maximum input ripple RMS current for a single output channel occurs at maximum load and can be estimated by:

$$I_{RMS(MAX)} \approx \frac{I_{LOAD(MAX)}}{V_{VIN}}\left[(V_{VOx})(V_{VIN}-V_{VOx})\right]^{1/2}$$

7.3.4 MOSFET Selection

The top and bottom MOSFET should be chosen for low $R_{DS(ON)}$ for increased efficiency, however this must be weighed with increased gate capacitance which increases switching losses. Switching losses are increased in the top MOSFET at high input voltages.

The bottom MOSFET should be placed in parallel with a Schottky diode. Many manufacturers provide a single package device

for the MOSFET and diode.

7.4 On-Demand Power® Operation

PSG5220 internal registers are programmable via SMBUS to control On-Demand Power® (ODP) circuitry. Activity on each domain is monitored by current sense and activity inputs. When the ODPEN bit of ODPxCON register is set, the corresponding output voltage will be managed based on configuration settings, signals on nACTx pins, and information gathered from current sensing circuits.

7.4.1 Output Voltage

Output voltage will vary based on system demand, managed by On-Demand Power® algorithms.

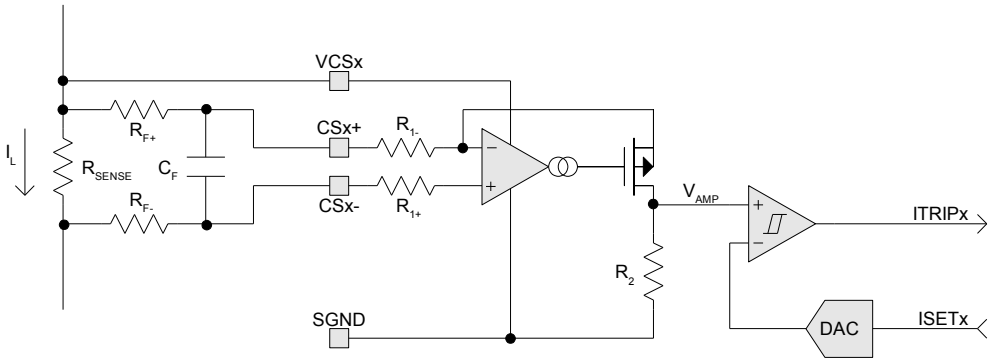
7.4.2 nACTx Inputs

nACT1 and nACT2 are system control inputs to the On-Demand Power® algorithm. A low signal on these pins indicate an instantaneous high power mode on the respective output channel. The algorithm will interpret this signal to immediately scale to the highest power, highest voltage state.

Both inputs are designed to operate on logic levels from 1.8V to 5V. They should be pulled up to 1.8V when used with SATA hard disk drives. Do not leave nACT1 or nACT2 floating. Pull-up to 1.8V when not in use.

7.4.3 Current Sense

The load current sense circuit detects if the load current I_L is above or below a programmable threshold I_{TRIP}. A high-side current sense amplifier gains the voltage V_{CS} across a sense resistor R_{SENSE} in response to the load current I_L. The output of the current sense amplifier is compared to a programmable threshold voltage V_{TRIP} that is set using an internal 8-bit DAC. The output of the comparator circuit is high if I_L is greater than I_{TRIP} and low if I_L is less than I_{TRIP}. The comparator includes internal hysteresis to help reject noise.



Current sense circuitry (one channel)

The load current sense resistor R_{SENSE} should be selected such that the maximum voltage drop $V_{cs(MAX)}$ across the sense resistor does not exceed the maximum differential input voltage of the current sense amplifier. For a maximum load current of I_{MAX}, the maximum value of R_{SENSE} is:

$$R_{SENSE(MAX)} = \frac{V_{CS(MAX)}}{I_{MAX}}$$

Likewise, the minimum value for R_{SENSE} depends on the minimum load current $I_{TRIP(MIN)}$ that must be detected:

$$R_{SENSE(MIN)} = \frac{V_{CS(MIN)}}{I_{TRIP(MIN)}}$$

The positive and negative sense traces should be routed as a differential pair and Kelvin connected to the sense resistor.

The inclusion of the input low-pass filter helps to smooth spiky load current and reduce the effects of capacitive and inductive noise coupled into the sense traces on the PCB. Adding a capacitor C_F between the CSx+ and CSx- pins in addition to the input resistors R_{F+} and R_{F-} forms a single pole low-pass differential filter with a cutoff frequency of:

$$f_C = \frac{1}{2\pi(R_{F+}+R_{F-})C_F}$$

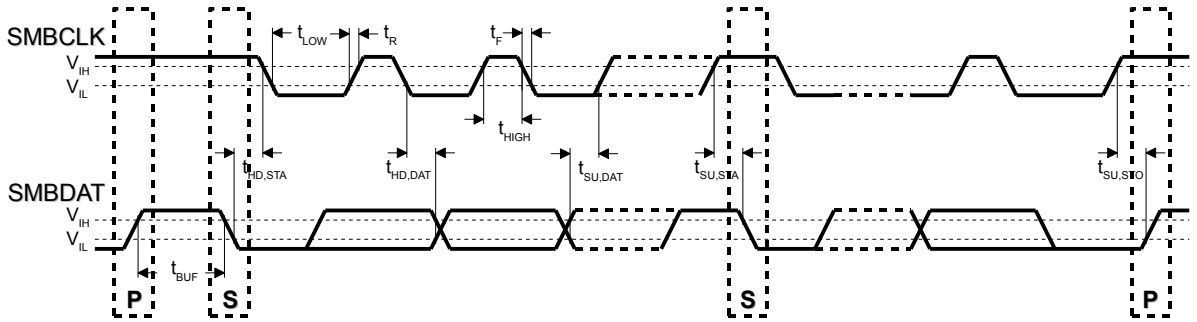
The additional amplifier input offset voltage induced by input resistors R_{F+} and R_{F-} is:

$$V_{OS} = I_{CS-}R_{F-} - I_{CS+}R_{F+}$$

7.5 SMBus Interface

The PSG5220 serial interface is SMBus 2.0 compliant. SMBCLK is the serial clock input and SMBDAT is the bidirectional serial data. PSG5220 is configured as a slave on the SMBus and has a fixed 7-bit slave address of 0x61. PSG5220 supports 'read byte', 'write byte', and 'block write' as described by the SMBus specification.

7.5.1 Timing Diagram



7.5.2 Address Map

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	NAME	DEFAULT VALUE
00H	*Reserved*								*Reserved*	*Reserved*
01H	*Reserved*								*Reserved*	*Reserved*
02H	*Reserved*								*Reserved*	*Reserved*
03H	AT_EN	*Reserved*			REGEN	ODD	*Reserved*	ODPEN	ODP1CON	0x08
04H	*Reserved*				AT_DN	*Reserved*			ODP1STAT	0x00
05H	Regulator 1 Manual Output Voltage								ODP1VMAN	0x00
06H	ODP1 Output Voltage 0								ODP1VOUT0	0x00
07H	ODP1 Output Voltage 1								ODP1VOUT1	0x00
08H	ODP1 Output Voltage 2								ODP1VOUT2	0x00
09H	ODP1 Output Voltage 3								ODP1VOUT3	0x00
0AH	Regulator 1 Manual Current Threshold								ODP1IMAN	0x00
0BH	ODP1 Current Threshold 0								ODP1ITH0	0x00
0CH	ODP1 Current Threshold 1								ODP1ITH1	0x00
0DH	ODP1 Current Threshold 2								ODP1ITH2	0x00
0EH	ODP1 Current Threshold 3								ODP1ITH3	0x00
0FH	Regulator 1 Rising Slew Rate								ODP1STEPUP	0x00
10H	Regulator 1 Falling Slew Rate								ODP1STEPDWN	0x00
11H	Regulator 1 Power Good Blank Time								ODP1PGBLANK	0x00
12H	ODP1 Timeout 0 [7:0]								ODP1TOUT0_0	0x00
13H	ODP1 Timeout 0 [15:8]								ODP1TOUT0_1	0x00
14H	ODP1 Timeout 0 [23:16]								ODP1TOUT0_2	0x00
15H	ODP1 Timeout 0 [31:24]								ODP1TOUT0_3	0x00
16H	ODP1 Timeout 1 [7:0]								ODP1TOUT1_0	0x00
17H	ODP1 Timeout 1 [15:8]								ODP1TOUT1_1	0x00
18H	ODP1 Timeout 1 [23:16]								ODP1TOUT1_2	0x00
19H	ODP1 Timeout 1 [31:24]								ODP1TOUT1_3	0x00
1AH	ODP1 Timeout 2 [7:0]								ODP1TOUT2_0	0x00
1BH	ODP1 Timeout 2 [15:8]								ODP1TOUT2_1	0x00
1CH	ODP1 Timeout 2 [23:16]								ODP1TOUT2_2	0x00
1DH	ODP1 Timeout 2 [31:24]								ODP1TOUT2_3	0x00

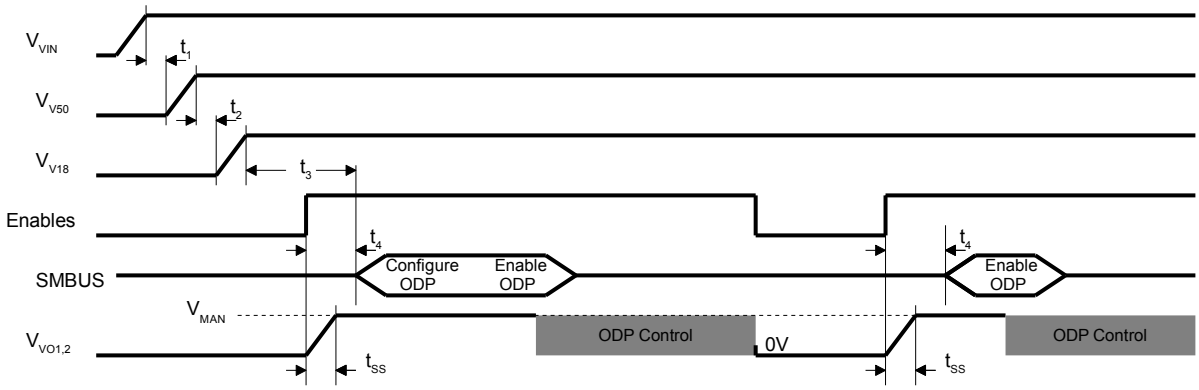
ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	NAME	DEFAULT VALUE
1EH	ODP1 Auto threshold count value								ODP1AT_CNT	0X00
1FH	ODP1 Initial Slew				ODP1 Initial Delay				ODP1TMRNSLEW	0X00
20H	*Reserved*								*Reserved*	*Reserved*
21H	*Reserved*								*Reserved*	*Reserved*
22H	AT_EN	*Reserved*			REGEN	ODD	*Reserved*	ODPEN	ODP2CON	0x08
23H	*Reserved*				AT_DN	*Reserved*			ODP2STAT	0x00
24H	Regulator 2 Manual Output Voltage								ODP2VMAN	0x00
25H	ODP2 Output Voltage 0								ODP2VOUT0	0x00
26H	ODP2 Output Voltage 1								ODP2VOUT1	0x00
27H	ODP2 Output Voltage 2								ODP2VOUT2	0x00
28H	ODP2 Output Voltage 3								ODP2VOUT3	0x00
29H	Regulator 2 Manual Current Threshold								ODP2IMAN	0x00
2AH	ODP2 Current Threshold 0								ODP2ITH0	0x00
2BH	ODP2 Current Threshold 1								ODP2ITH1	0x00
2CH	ODP2 Current Threshold 2								ODP2ITH2	0x00
2DH	ODP2 Current Threshold 3								ODP2ITH3	0x00
2EH	Regulator 2 Rising Slew Rate								ODP2STEPUP	0x00
2FH	Regulator 2 Falling Slew Rate								ODP2STEPDWN	0x00
30H	Regulator 2 Power Good Blank Time								ODP2PGBLANK	0x00
31H	ODP2 Timeout 0 [7:0]								ODP2TOUT0_0	0x00
32H	ODP2 Timeout 0 [15:8]								ODP2TOUT0_1	0x00
33H	ODP2 Timeout 0 [23:16]								ODP2TOUT0_2	0x00
34H	ODP2 Timeout 0 [31:24]								ODP2TOUT0_3	0x00
35H	ODP2 Timeout 1 [7:0]								ODP2TOUT1_0	0x00
36H	ODP2 Timeout 1 [15:8]								ODP2TOUT1_1	0x00
37H	ODP2 Timeout 1 [23:16]								ODP2TOUT1_2	0x00
38H	ODP2 Timeout 1 [31:24]								ODP2TOUT1_3	0x00
39H	ODP2 Timeout 2 [7:0]								ODP2TOUT2_0	0x00
3AH	ODP2 Timeout 2 [15:8]								ODP2TOUT2_1	0x00
3BH	ODP2 Timeout 2 [23:16]								ODP2TOUT2_2	0x00
3CH	ODP2 Timeout 2 [31:24]								ODP2TOUT2_3	0x00
3DH	ODP2 Auto threshold count value								ODP2AT_CNT	0x00
3EH	ODP2 Initial Slew				ODP2 Initial Delay				ODP2TMRNSLEW	0X00
3FH	*Reserved*								*Reserved*	*Reserved*
40H	*Reserved*								*Reserved*	*Reserved*
41H	4'h0				OCPROG[3:0]				VREG1_CON	0x00
42H	4'h0				OCPROG[3:0]				VREG2_CON	0x00
43H	ANA2 EN_STAT	PG2 STAT	OVP2 STAT	UVP2 STAT	ANA1 EN_STAT	PG1 STAT	OVP1 STAT	UVP1 STAT	VREGSTAT	0x00
44H-FFH	*Reserved*								*Reserved*	*Reserved*

7.6 Operating Sequence

A typical control sequence for the PSG5220 is:

- Apply V_{VIN} and V_{V50} Note: V_{VIN} needs to be powered before V_{V50}
- V_{V18} is supplied from the internal 1.8V LDO
- Enable PSG5220
- Configure ODP control of PSG5220 through SMBUS
- Optionally configure V_{MAN} to another voltage by writing to ODPxVMAN. Output voltage will change immediately.

- Enable ODP by writing 1 to ODPEN of ODPxCON. Output voltage will be under ODP control immediately.
- SMBUS will not operate before t_3 and t_4 have expired.



Start-up sequence minimum timings:

- t_1 = 0s
- t_2 = 0s
- t_3 = 250us
- t_4 = 250us
- t_{SS} = 1.5ms

Power Down Sequence: Remove V_{V50} before V_{VIN}.

7.7 Typical Applications

7.7.1 Application – Intel Mobile Platform

The PSG5220 is well suited for use into the Intel mobile platform. Appropriate connections must be made by the system designer for connection to the mainboard power delivery system, bus architecture, and to hard-disk drives (HDD) and optical-disk drives (ODD). For optimal performance, the current sense resistor and current sense circuitry of each channel should be sized appropriately for the type of drive that will be powered by the channel. For example, a smaller sense resistor should be used for a higher power drive to ensure the input differential voltage of the current sense circuit remains in the working range.

Connections to Power

Description	Voltage	PSG5220 Lead	Intel Mobile Platform
Analog Input Supply Voltage	5V	V50	V5.0A
Input Voltage	6.5V to 24V	VIN	Battery/Brick
I/O Voltage	5V	VDDIO	V5.0A
Digital Input Supply Voltage	1.8V	V18	N/A

The switching regulator input voltage is supplied from the battery/brick input voltage to the mobile platform. Since the PSG5220 supports a very wide input range, the system is not required to support narrow voltage direct current (NVDC).

Analog circuitry in the PSG5220 operates at 5V. It is required that this be supplied externally and remain 'ON' in all operational and sleep states. Connect this to V5.0A.

The I/O for the PSG5220 are designed to operate at 5V. Connect these to V5.0A.

Internal digital logic is powered at 1.8V. The PSG5220 supplies this voltage through an internal LDO and should not be connected to an external 1.8V supply. The LDO output, LDO1V8, must be connected to VDD and be appropriately decoupled as described in this document.

Connections to I/O

The PSG5220 manages the voltage supplied to the drives based on information gathered from sensing current and activity feedback on the bus. nACT1 and nACT2 provide activity information from HDD devices to PowerSage®. HDD devices should support the optional activity indication on pin P11 of the SATA power connector. Connect the activity indicator signal to nACT with a 10k pull-up resistor to 1.8V at LDO1V8. The PSG5220 will operate without the nACT signal on HDD devices but will provide less energy savings. Do not leave nACT floating. Pull-up to LDO1V8 when not in use. nACT is left unconnected for ODD devices.

Communication to the register map is provided through the SMBus interface through pins SMBDAT and SMBCLK. System designers can choose to connect this directly to the Platform Controller Hub (PCH) or through an SMBus hub. The SMBus pull-up resistors should be connected to 3.3V through V3.3A or V3.3S.

Configuration Registers

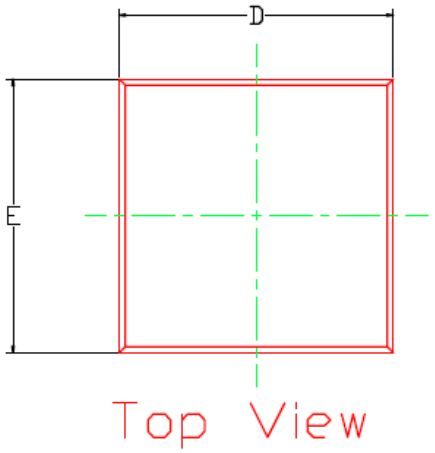
A number of configuration registers must be set for the PowerSage® logic to run properly in PSG5220. Voltage, threshold, and timeout registers can be set through the SMBus interface. Packet Digital can supply the appropriate configurations for specific HDD and ODD devices. Additionally, an automatic configuration program is scheduled to be available on future releases.

8 Mechanical Information

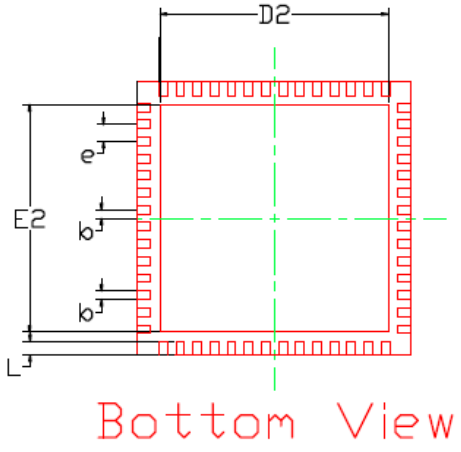
8.1 VLD Package

56-Lead Plastic QFN (8mm X 8mm)

All dimensions are in millimeters unless otherwise noted.



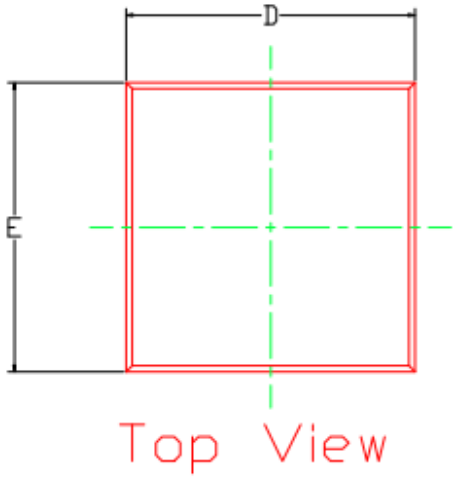
DIMENSION (mm)			
SYMBOL	MIN	NOM	MAX
A	0.8000	0.850	0.9000
A3		0.200	
b	0.180	0.250	0.300
D		8.000	
D2	6.500	6.650	6.800
E		8.000	
E2	6.500	6.650	6.800
e		0.500	
L	0.350	0.400	0.450
θ	0 deg.		14 deg.



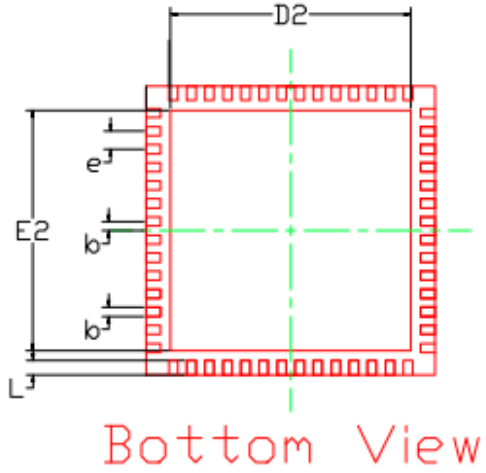
8.2 VKE Package

56-Lead Plastic QFN (7mm X 7mm)

All dimensions are in millimeters unless otherwise noted.



DIMENSION (mm)			
SYMBOL	MIN	NOM	MAX
A	0.8000	0.850	0.9000
A3		0.200	
b	0.150	0.200	0.250
D		7.000	
D2	4.950	5.100	5.250
E		7.000	
E2	4.950	5.100	5.250
e		0.400	
L	0.300	0.400	0.500
θ	0 deg.		14 deg.



9 Reference Circuit

#	QTY	REFDES	Value	Description	PKG_TYPE	MFG	MFG-PN
1	1	R7	1	RES, 1R, 0.063W, 5%, 0402, TKF	402	PANASONIC	ERJ-2GEJ1R0X
2	1	C36	0.1u	CAP, 0.1UF, 50V, CER, X7R, 0603	603	PANASONIC	ECJ-1VB1H104K
3	1	C30	10u	CAP, 10UF, 6.3V, CER, X5R, 20%, 0603	603	TDK	C1608X5R0J106M
4	1	U1		POWERSAGE PETTIBONE, QFN-56_MO-220WLLD_DATASHEET	QFN-56_MO-220WLLD	PACKET DIGITAL	PSG5220
5	2	R12-R13	100	RES, 100R, 0.063W, 5%, 0402, TKF	402	PANASONIC	ERJ-2GEJ101X
6	2	R14-R15	133	RES, 133R, 0.063W, 1%, 0402, TKF	402	PANASONIC	ERJ-2RKF1330X
7	2	R8-R9	0.04	RES, 0.04, 3W, 1%, SMT	2512	BOURNS	CRA2512-FZ-R040ELF
8	2	C27-C28	0.001u	CAP, 1000PF, 50V, CER, X7R, 0402	402	PANASONIC	ECJ-0EB1H102K
9	2	C32, C34	0.01u	CAP, 10000PF, 50V, CER, X7R, 0603	603	PANASONIC	ECJ-1VB1H103K
10	2	C12, C14	2.2u	CAP, 2.2UF, 10V, CER, X5R, 0603	603	PANASONIC	ECJ-1VB1A225K
11	2	C10-C11	100u	CAP, 100UF, 6.3V, TANT, 20%, 3528-21	3528-21	KEMET	T520B107M006ATE025
12	2	D1-D2		DIODE, SCHOTTKY, 30V, 200MA, SOT23-3_TO-236AB	SOT23-3_TO-236AB	FAIRCHILD	BAT54C
13	2	Q1-Q2		Q, NMOS, DUAL, 30V, 6.3A, SHUNT SCHOTTKY, SOIC-8_150MIL_MS-012AA	SOIC-8_150MIL	FAIRCHILD	FDS6982AS
14	2	L1-L2	3.3u	IND, 3.3UH, 14A, SMD	XPL7030	COILCRAFT	XPL7030-332ML_
15	3	R6, R10-R11	10K	RES, 10K, 0.063W, 1%, 0402, TKF	402	YAGEO	RC0402FR-0710KL
16	3	C29, C31, C33	1u	CAP, 1UF, 50V, CER, 10%, X5R, 0603	603	TAIYO YUDEN	UMK107BJ105KA-T
17	4	C16-C17, C37-C38	10u	CAP, 10UF, 35V, CER, X5R, 1210	1210	TAIYO YUDEN	GMK325BJ106KN
18	5	C4-C5, C7, C9, C21	4.7u	CAP, 4.7UF, 6.3V, CER, X5R, 10%, 0603	603	TDK	C1608X5R0J475K
19	8	C13, C15, C20, C22-C26	0.1u	CAP, 0.1UF, 16V, CER, X5R, 0402	402	PANASONIC	ECJ-0EB1C104K