Evaluation Board for Constant-Frequency, Current-Mode, Step-Up, DC/DC Controller

EVAL-ADP1621

EVALUATION BOARD DESCRIPTION

This data sheet describes the design, operation and test results of the ADP1621 Evaluation Board. The input range for the demo board is 3.0 V to 3.6 V, and the output voltage is 5 V with a maximum load of 2 A. The design is done in a bootstrapped configuration as shown in Figure 13. The switching frequency f_{SW} is set to 600 kHz with a 36 kΩ resistor. This design is done in all multilayer ceramic capacitors (MLCC), although other types of capacitors can be used, such as the aluminum polymer or aluminum electrolytic capacitors. The PCB is laid out in such a way that the user can easily modify the demo board for other input and output configurations. See the Other Configurations section for more information.

ADP1621 DEVICE DESCRIPTION

The ADP1621 is a fixed-frequency, pulse-width modulation (PWM), current-mode, step-up converter controller. It drives an external n-channel MOSFET to convert the input voltage to a higher output voltage. The ADP1621 can also be used to drive flyback, SEPIC, and forward converter topologies, either isolated or nonisolated.

EVALUATION BOARD

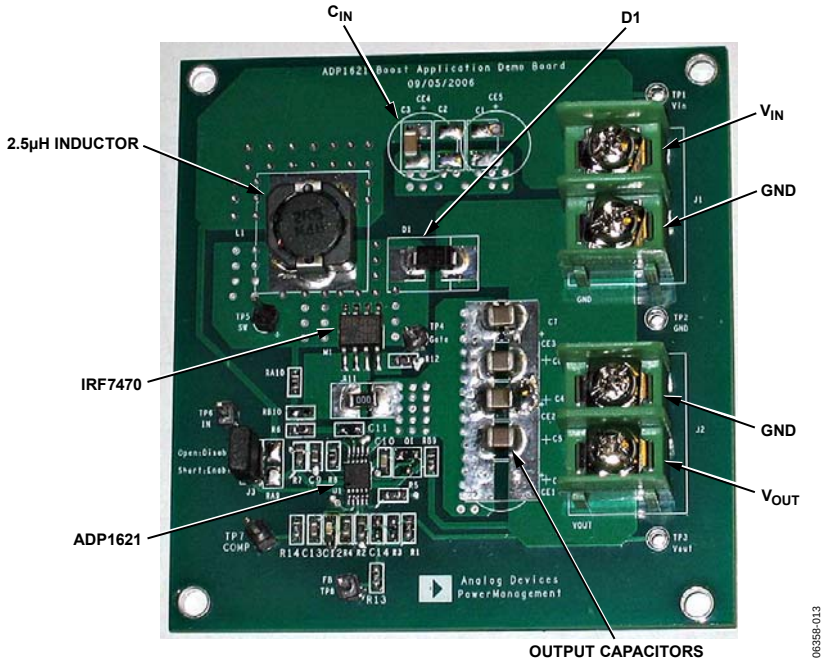

Figure 1.

Rev. 0

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REVISION HISTORY

11/06—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

Table 1. Jumper Description

Jumper	Description	Function
J1	V_{IN} and GND terminals	
J2	V_{OUT} and GND terminals	
J3	SDSN connection	Connects SDSN to V_{IN} or drives SDSN separately

Table 2. Demo Board Specifications

Parameter	Description
V_{IN}	Input range , 3.0 V to 3.6 V
V_{OUT}	5 V
f_{SW}	Switching frequency, 600 kHz
Efficiency	90% at 1 A load
Maximum Load	2 A
Duty Cycle	40% (V_{IN} = 3.3 V)
Output Ripple	30 mV with 1 A load at 25°C
Input Ripple	25 mV at 25°C

COMPONENT SELECTION

For more information about component selection, refer to the ADP1621 data sheet available. Consult the ADP1621 data sheet in conjunction with this data sheet when using the evaluation board.

Duty Cycle

$$D = \frac{V_{OUT} + V_D - V_{IN}}{V_{OUT} + V_D} \quad (1)$$

where:

V_{OUT} is the desired output voltage.
V_{IN} is the input voltage.
V_D is the forward-voltage drop of the diode.

With V_{IN} = 3.3 V, and V_{OUT} = 5 V, the duty cycle is calculated to be about 40%, assuming V_D is about 0.5 V.

Feedback Resistors

$$V_{OUT} = 1.215\ \text{V} \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

With V_{OUT} = 5 V and if R2 = 5.6 kΩ, then R1 is calculated to be 17.4 kΩ.

Inductor Selection

The average inductor current, $I_{L,AVE}$, is given by

$$I_{L,AVE} = \frac{I_{LOAD}}{1-D} \quad (3)$$

where I_{LOAD} is the load current.

With I_{LOAD} = 2 A and D = 0.4, $I_{L,AVE}$ is calculated to be 3.33 A. To reduce the size of the inductor and to minimize the output bulk capacitance, set the switching frequency f_{SW} to 600 kHz. Assuming a 30% ripple current of 1/(1 − D) × 2 A (the load current) in the inductor, the inductor value is calculated from the following equation:

$$L = \frac{V_{IN} \times D \times (1-D)}{0.3 \times f_{SW} \times I_{LOAD,MAX}} \quad (4)$$

L is then calculated to be 2.2 µH. For this demo board, a 2.5 µH is selected. Make sure that the selected inductor can handle the average dc current of 3.33 A and a peak current of at least 4 A, which is given by

$$I_{L,PK} = \frac{I_{LOAD}}{1-D} + \frac{\Delta I_L}{2} = \frac{I_{LOAD}}{1-D} + \frac{V_{IN} \times D}{2 \times f_{SW} \times L} \quad (5)$$

Input Capacitor Selection

Because ceramic capacitors have very low ESR. (a few mΩ), a 47 µF, 6.3 V Murata GRM31CR60J476M (size 1206) ceramic capacitor is chosen for the input capacitor. If the load current gets larger than 2 A, a larger input capacitor is needed to reduce the input ripples current. Other types of input capacitors with higher ESR can be used, such as the aluminum electrolytic or the aluminum polymer types. Make sure the ripple current rating of the input capacitor, $I_{CIN,RMS}$, is greater than

$$I_{CIN,RMS} = \frac{1}{\sqrt{3}} \times \frac{\Delta I_L}{2} \quad (6)$$

where ΔI_L is the peak-to-peak inductor ripple current.

Output Capacitor Selection

The output voltage ripple for a given C_{OUT}, ESR, and ESL, the effective equivalent series inductance of C_{OUT}, can be found by solving the following equation:

$$\Delta V_{OUT} \approx \left(\frac{I_{LOAD}}{1-D} + \frac{\Delta I_L}{2}\right) \times \sqrt{\left(\frac{1}{2\pi \times f_{SW} \times C_{OUT}}\right)^2 + ESR^2 + \left(2\pi \times f_{SW} \times ESL\right)^2} \quad (7)$$

By setting an output voltage ripple equal to 1% (50 mV) of the output voltage, Equation 7 yields that the minimum C_{OUT} required is 20 µF by using an ESR of 2 mΩ and an ESL of 100 nH. The effective capacitance of a ceramic capacitor generally decreases with increasing bias voltage and with smaller casings in the same bias voltage. For the demo board, four 10 µF/16 V (size 1210) ceramic capacitors were selected. Other combinations of capacitance and ESR are possible by choosing a much larger C_{OUT} with a larger ESR.

Diode Selection

The diode conducts the inductor current to the output capacitor and loads while the MOSFET is off. The average diode current is the load current,

$$I_{DIODE,AVE} = I_{LOAD} \quad (8)$$

The rms diode current in continuous conduction mode is given by

$$I_{DIODE,RMS} = \frac{I_{LOAD}}{1-D} \times \sqrt{1-D} \quad (9)$$

where D is the duty cycle.

With a 2 A load, $I_{DIODE,RMS}$ is calculated to be 2.6 A. A Vishay SSA33L in a SMA package meets the dc current and thermal requirements.

MOSFET Selection

The power MOSFET must be chosen based on threshold voltage (V_T), on resistance (R_{DSON}), maximum voltage and current ratings, and gate charge. The RMS current through the MOSFET is given by the following equation:

$$I_{RMS,MOSFET} = \frac{I_{LOAD}}{1-D} \times \sqrt{D} \quad (10)$$

where $I_{RMS,MOSFET}$ is calculated to be 2.1 A, assuming I_{LOAD} is 2 A and D is 0.4.

The IRF7470 is a 40 V n-channel power MOSFET that meets the current and thermal requirements. It comes in an 8-lead SOIC package and offers low R_{DSON} and gate charge. R_{DSON} is 30 mΩ at V_{GS} = 2.8 V and 15 mΩ at V_{GS} = 4.5 V. This general-purpose MOSFET meets a wide range of output voltage and current requirements. An alternative to this part is the Vishay Si7883DP, a 20 V n-channel power MOSFET.

Loop Compensation

The location of the right hand plane (RHP) zero frequency is determined by the following equation:

$$f_{Z,RHP} = (1-D)^2 \times \frac{R_{LOAD}}{2\pi \times L} \quad (11)$$

where:

$f_{Z,RHP}$ is the RHP zero frequency.
R_{LOAD} is the equivalent load resistance, or the output voltage divided by the load current.

To stabilize the regulator, ensure that the regulator crossover frequency is ≤1/5th of the RHP zero frequency and ≤1/15th of the switching frequency. With V_{OUT} = 5 V at 2 A load, $f_{Z,RHP}$ is calculated to be 57.3 kHz.

For an initial practical design, set the crossover frequency f_C to the lower frequency of

$$f_C = \frac{f_{SW}}{15} \quad (12)$$

and

$$f_C = \frac{f_{Z,RHP}}{5} \quad (13)$$

where:

f_C is the crossover frequency.
f_{SW} is the switching frequency.

Equation 13 shows that f_C is 40 kHz and is lower frequency than that of Equation 12. The loop compensation components are calculated to be R_{COMP} = 33 kΩ and C_{COMP} = 490 pF from Equation 14 and Equation 15, respectively. The final component values need to be tested and verified on the actual PCB.

R_{COMP} is given by

$$R_{COMP} = \frac{2\pi \times f_C \times C_{OUT} \times n \times R_{CS} \times V_{OUT}}{V_{FB} \times (1-D) \times g_m} \quad (14)$$

where:

V_{FB} = 1.215 V
D = 0.4
g_m = 300 µS
R_{CS} = 15 mΩ for the IRF7470 at V_{GS} = 4.5 V
V_{OUT} = 5 V
n = 9.5 (typically)
C_{OUT} ≈ 40 µF
f_C = 40 kHz (f_{SW}/15 = 60 kHz/15).

To fine-tune the R_{COMP} and C_{COMP} values on the evaluation board, run a step load, for example, from 0.2 A to 1 A, at the output and observe the output transient. If there is too much overshoot in the transient, increase R_{COMP}; if there is too much oscillation, increase C_{COMP}.

Once the compensation resistor R_{COMP} is known, set the zero formed by the resistor and compensation capacitor C_{COMP} to 1/4th of the crossover frequency, or

$$C_{COMP} = \frac{2}{\pi \times f_C \times R_{COMP}} \quad (15)$$

A roll-off capacitor of C2 = 390 pF is also added on the demo board. A smaller C2 works fine.

Slope Compensation

The slope-compensation resistor R_S = 142 Ω from the following equation:

$$R_S > \frac{R_{CS} \times (V_{OUT} + V_D - V_{IN}) \times (1 - t_{OFF,MIN} \times f_{SW})}{2 \times I_{SC,PK} \times f_{SW} \times L} \quad (16)$$

where:

$t_{OFF,MIN}$ = 230 ns
f_{SW} = 600 kHz
L = 2.5 µH
$I_{SC,PK}$ = 70 µA.

Current Limit

The current limit in the ADP1621 limits the peak inductor current and is achieved by the COMP voltage clamp. The peak inductor current, $I_{L,PK}$, is given by

$$I_{L,PK} = \frac{\frac{V_{COMP,CLAMP} - V_{COMP,ZCT}}{n} - \frac{I_{SC,PK} \times R_S \times D}{1 - t_{OFF,MIN} \times f_{SW}}}{R_{CS}} \quad (17)$$

where:

$V_{COMP,CLAMP}$ is the COMP clamp voltage (maximum 2.1 V).
$V_{COMP,ZCT}$ is the COMP zero-current threshold (typically 1.0 V).
n is the current-sense amplifier gain (typically 9.5).
$I_{SC,PK}$ is the peak slope-compensation current (typically 70 µA).
R_S is the slope-compensation resistor.
D is the duty cycle.
f_{SW} is the switching frequency.
$t_{OFF,MIN}$ is the minimum off time (typically 190 ns).
R_{CS} is the current-sense resistor.

The peak inductor current limit also limits the maximum load current at a given output voltage. The maximum load current, assuming continuous conduction mode (CCM) operation, is given by

$$I_{LOAD,MAX} = (1 - D) \times \left(\frac{\frac{V_{COMP,CLAMP} - V_{COMP,ZCT}}{n} - \frac{I_{SC,PK} \times R_S \times D}{1 - t_{OFF,MIN} \times f_{SW}}}{R_{CS}} - \frac{V_{IN} \times D}{2 \times f_{SW} \times L} \right) \quad (18)$$

where:

n = 9.5
$V_{COM,CLAMP}$ = 2.1 V
$V_{COMP,ZCT}$ = 1.0 V.

The current limit, $I_{LOAD,MAX,}$ is calculated to be ~4 A for this demo board. Note that the diode SSA33L is not rated for continuous current operation at 4 A. The maximum load current for this demo board is designed for 2 A.

Note that the current limit in the ADP1621 is a soft current limit. When the inductor current reaches the $I_{L,PK}$ limit given in Equation 17, the duty cycle decreases, and the output voltage drops below the desired voltage. The $I_{L,PK}$ limit then increases in response to the smaller duty cycle, D. The larger the slope-compensation resistor (R_S), the larger the effect on $I_{L,PK}$ for an incremental decrease in D. This behavior results in a soft current limit for the ADP1621. Use values of R_S that are as close as possible to the calculated limit derived from Equation 16 to minimize the softness of the current limit while maintaining current-loop stability. If high-precision current limiting is required, consider inserting a fuse in series with the inductor.

Power Components

See Table 3 for the temperature of the power components after running the board at a 2 A load for 30 minutes.

T_A = 22°C

Table 3.

Power Component	T(°C)
2.5 µH Inductor	34
MOSFET IRF7470	44
ADP1621	32

TEST WAVEFORMS

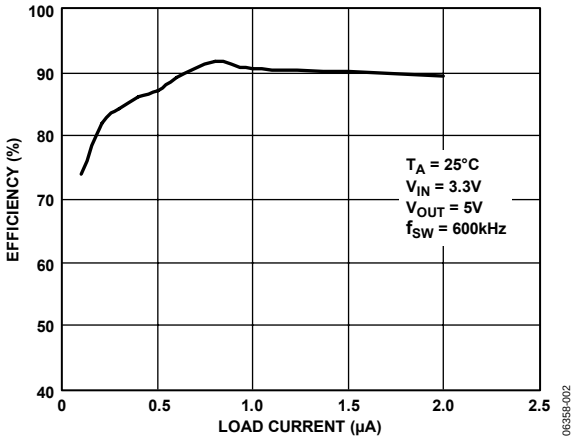

Figure 2. Efficiency vs. Load Current

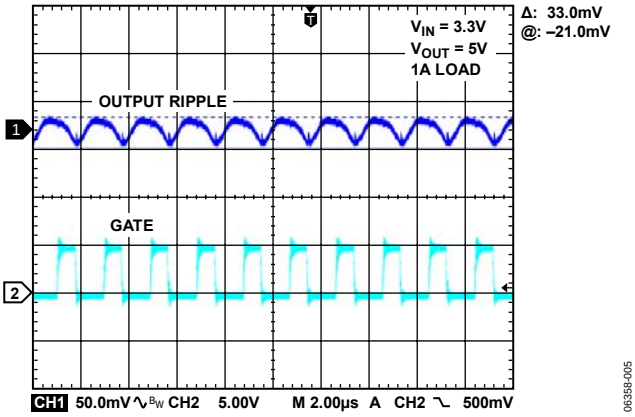

Figure 5. Output Voltage Ripple, 1 A Load

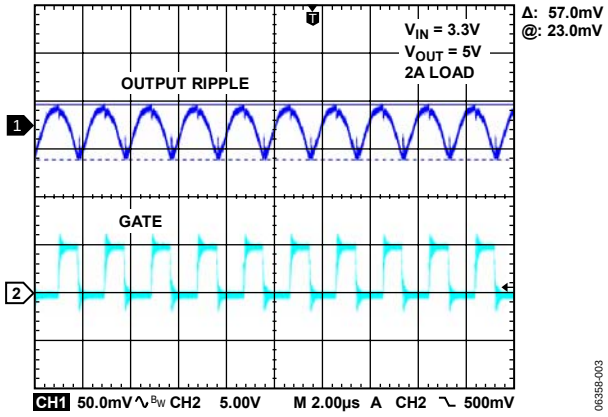

Figure 3. Output Voltage Ripple, 2 A Load

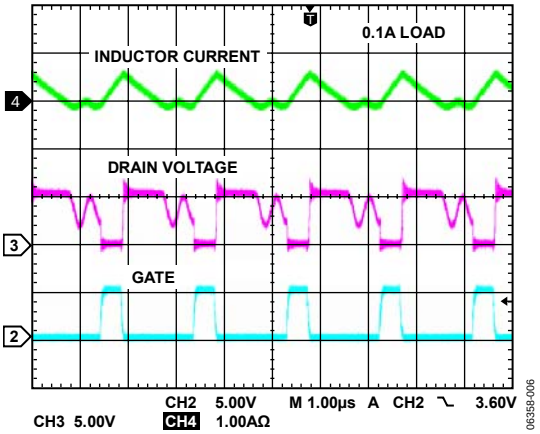

Figure 6. DCM Switching Waveform, 0.1 A Load

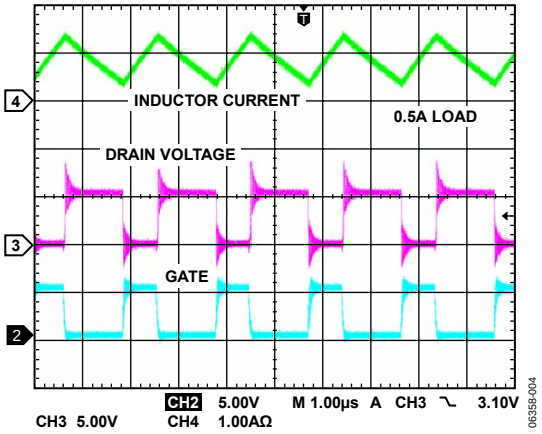

Figure 4. CCM Switching Waveform, 0.5 A Load

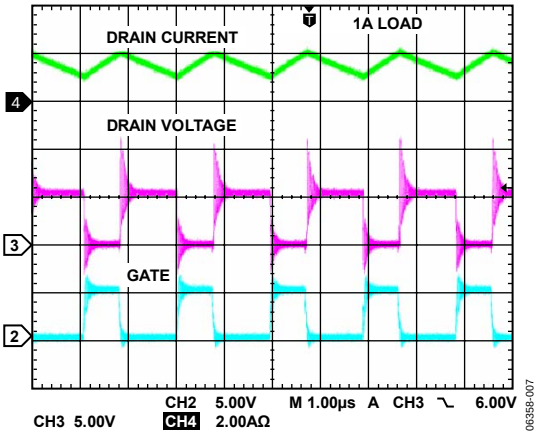

Figure 7. CCM Switching Waveform, 1 A Load

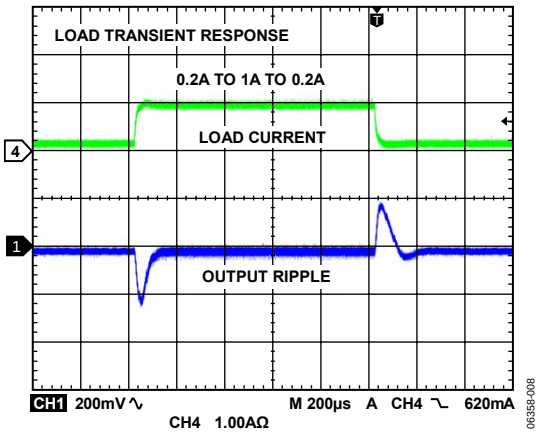

Figure 8. Load Transient Response

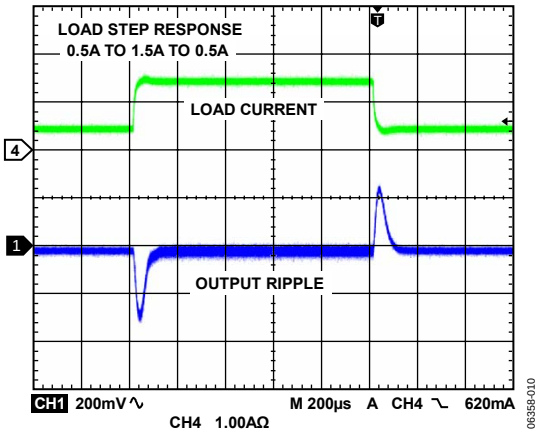

Figure 10. Load Step Response

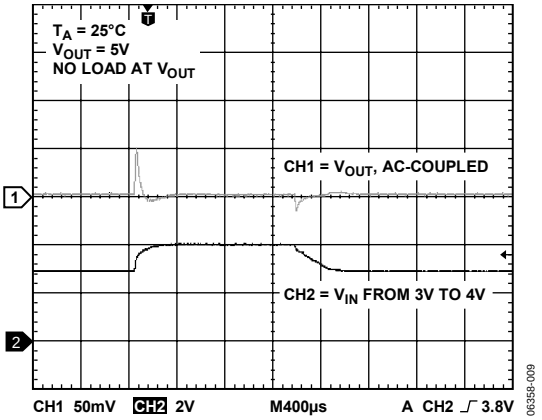

Figure 9. Line Transient Response with No Load

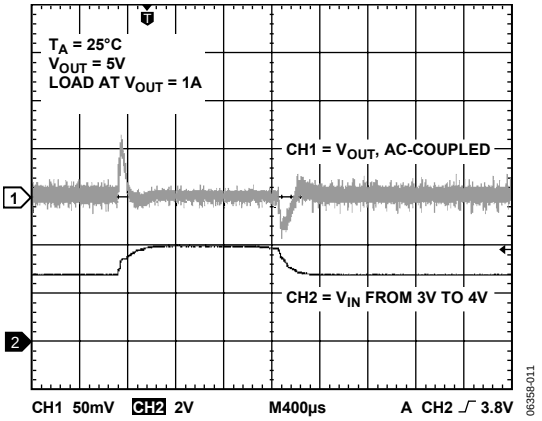

Figure 11. Line Transient Response with a 1 A Load

PCB LAYOUT GUIDELINE

Layout is important for all switching regulators, but is particularly important for regulators with high switching frequencies. To achieve high efficiency, good regulation, and stability, a well-designed printed circuit board layout is required. A sample 2-layer PCB layout for the standard boost converter circuit is shown in Figure 12.

Follow these guidelines when designing printed circuit boards:

- Keep the low ESR input capacitor, C_{IN}, close to IN, PIN and PGND.
- Keep the high current path from C_{IN} through Inductor L1 and MOSFET M1 to PGND as short as possible.
- Keep the high current path from C_{IN} through Inductor L1, Diode D1, and Output Capacitor C_{OUT} as short as possible.
- Keep high current traces as short and wide as possible to minimize parasitic series inductance, which causes spiking and electromagnetic interference (EMI).
- Place the feedback resistors as close to FB as possible to prevent high frequency switching-noise injection.
- Place the top of the upper feedback resistor, R1, as close as possible to the top of C_{OUT} for optimum output voltage sensing.
- If a current-sense resistor is connected between the source of the MOSFET and PGND, ensure that the capacitance from CS to PGND is minimized.
- Place the compensation components as close as possible to COMP.
- To minimize switching noise, the drain of the power MOSFET should be placed very close to the inductor, and the source of the MOSFET (or the bottom side of the sense resistor) should be connected directly to the power GND plane. Use wide copper traces on the drain and on the source of the MOSFET to minimize parasitic inductance and resistance. Parasitic inductance can lead to excessive ringing during switching transitions, and parasitic resistance reduces the converter efficiency. Make sure that the MOSFET selected is capable of handling total power loss (conduction plus transition losses) in the application circuit.
- Avoid routing high impedance traces near any node connected to the switch node (the MOSFET drain) or near Inductor L1 to prevent radiated switching-noise injection.
- Add an extra copper plane at the connection of the MOSFET drain and the anode of the diode to help dissipate the heat generated by losses in those components.
- Avoid ground loops by having one central ground node on the PCB. If this is impractical, place the power ground with high current levels physically closer to the PCB ground terminal. The analog, low current-level ground should be placed farther from the PCB ground terminal.
- Minimize the length of the PCB trace between the GATE pin and the MOSFET gate. The parasitic inductance in this PCB trace can give rise to excessive voltage ringing at the drain and the output. It is recommended to add 5 Ω of resistance for every inch of PCB trace. This helps to reduce the overshoot and ringing at the drain and the output. However, this added resistance increases the rise and fall times of the MOSFET; thus, the switching loss in the MOSFET is increased.

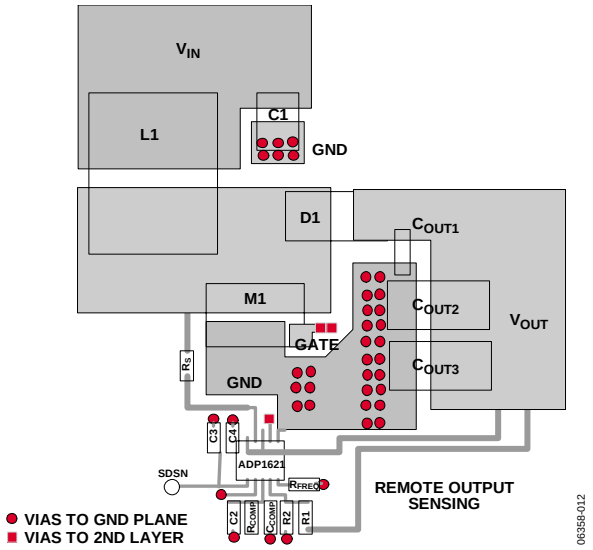

Figure 12. Boost Converter Layout (2-layer PCB)

OTHER CONFIGURATIONS

The demo board can be easily modified for other input voltage and output voltage options.

- For a nonbootstrapping configuration, assemble RA9 = 0 Ω, and remove RB9.
- For input voltages higher than 6 V, an NPN transistor Q1 and R7 can be assembled to form an LDO that brings down the input voltage down to 5 V to power the ADP1621. Alternatively, RA9 can be used to bring down the input voltage to the shunt regulation voltage, V_{SHUNT}. The drawback in using a large RA9 resistor is the higher power dissipation in this resistor when driving a large MOSFET or when the input voltage range is large.
- For output voltages higher than 28 V, connect the CS pin to the current sense resistor R11. On the current demo board version, R11 is a 0 Ω resistor. Make sure the MOSFET V_{DS} is rated for at least 40 V.
- The surface-mount ceramic capacitors are used on this demo board; other types of bulk input and output capacitors can also be used. The board is laid out to accommodate the surface-mount aluminum polymer and the through-hole aluminum electrolytic capacitors.

EVALUATION BOARD SCHEMATIC AND ARTWORK

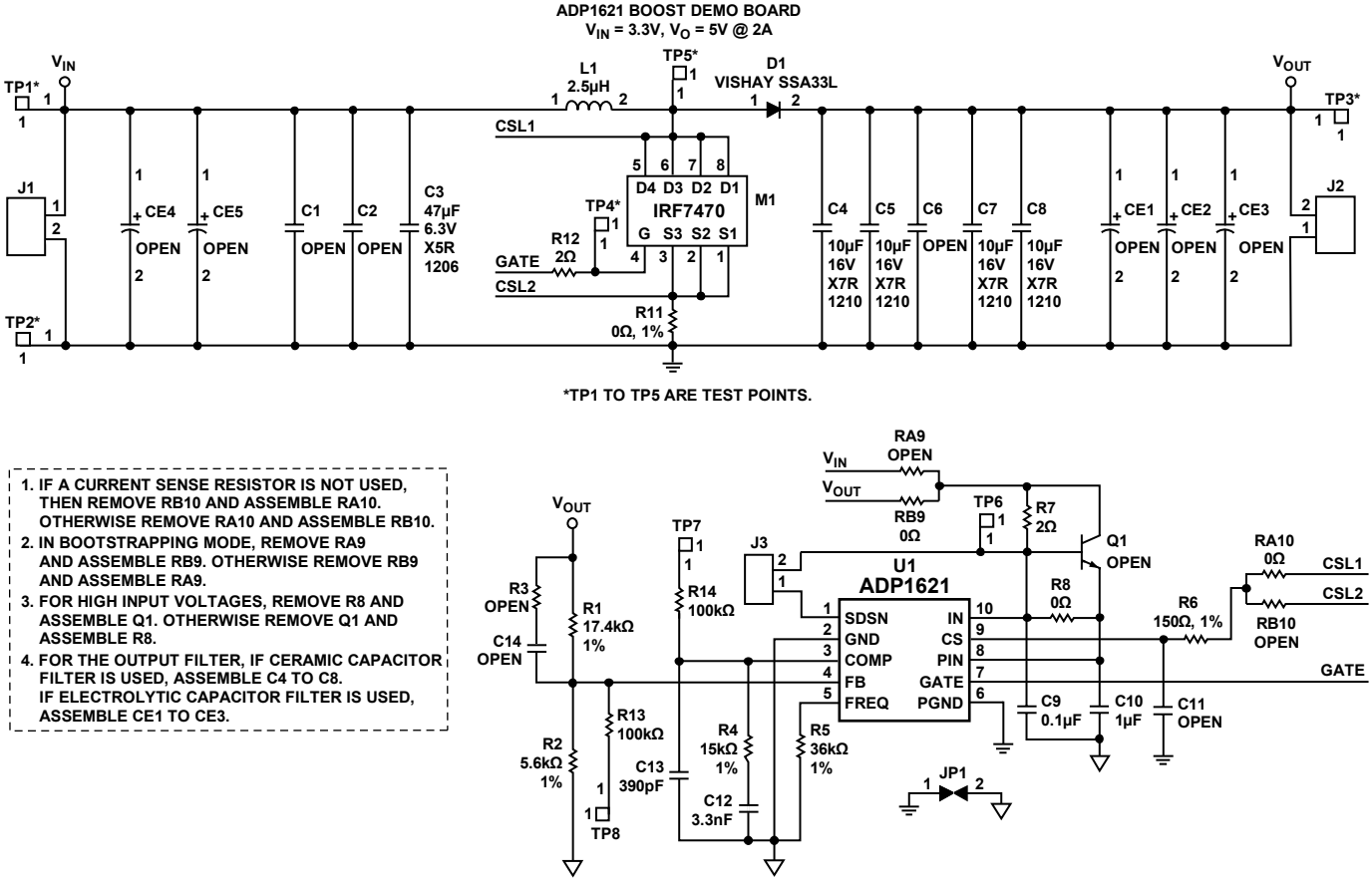

Figure 13. ADP1621 Evaluation Board Schematic

PCB LAYOUT

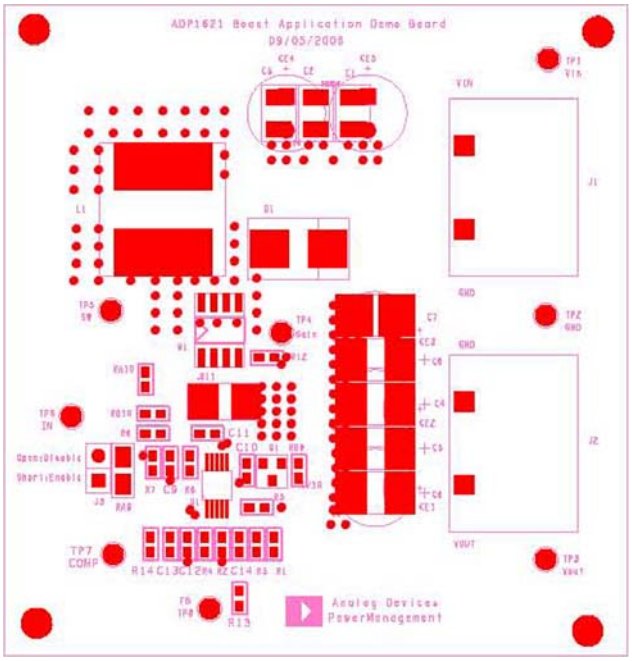

Figure 14. Silk Screen

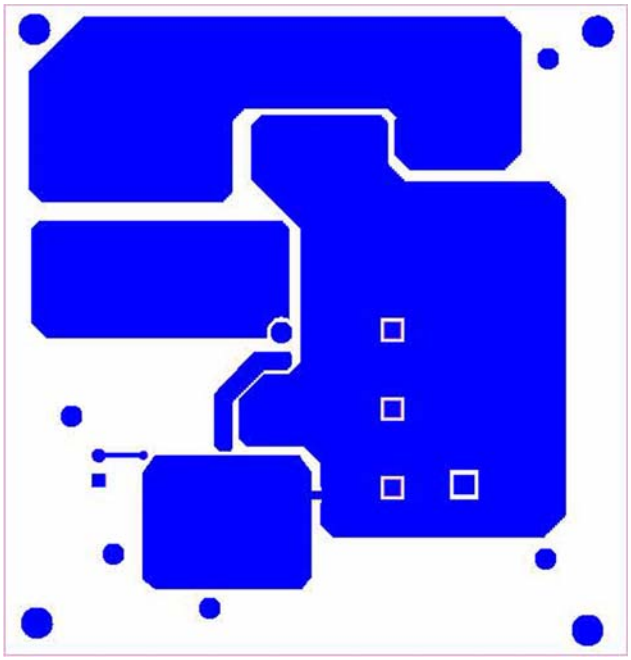

Figure 16. Bottom Layer

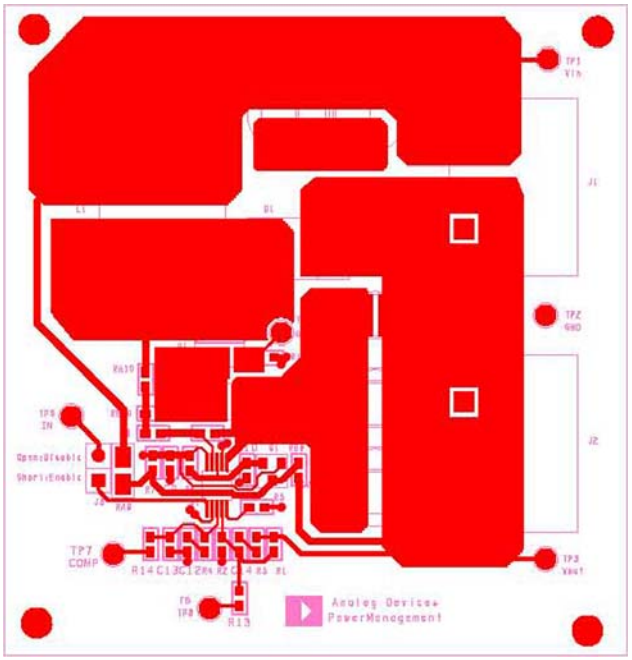

Figure 15. Top Layer

ORDERING INFORMATION

BILL OF MATERIALS

The ADP1621 evaluation board schematic is shown in Figure 13. Table 4 shows the bill of materials of the evaluation board.

V_{IN} = 3.0 V to 3.6 V, V_{OUT} = 5 V, I_{OUT} = 2 A, bootstrapped configuration.

Table 4.

Qty	Reference Designator	Description	Supplier	Supplier Number
1	M1	MOSFET, 8 L SOIC, 40 V, V_{GS} = 2.8 V, 5 A, 15 mΩ @ 4.5 V_{GS}, 30 mΩ @2.8 V_{GS}	IRF	IRF7470
1	D1	Schottky, 3 A, 30 V, SMA	Vishay	SSA33L
1	L1	2.5 µH inductor, shielded, 7.5 A Isat, 11 mΩ	Sumida or Coilcraft®	CDRH104R-2R5NC or MSS1038-252NL
1	C3	Capacitor, MLCC, 47 µF, 6.3 V, X5R, 1206	Murata	GRM31CR60J476M
4	C4, C5, C7, C8	Ceramic capacitor, 10 µF, 16 V, X7R, 1210	Murata	GRM32DR71C106KA01
1	C9	Capacitor, MLCC, 0.1 µF, 10 V, 0603, X5R	Murata or Vishay	VJ0603Y104MXQ
1	C10	Capacitor, MLCC, 1 µF, 10 V, 0603, X5R	Murata	GRM188R61A105K
1	C12	Capacitor, MLCC, 3.3 nF, 0603	Vishay	VJ0603Y332KXXA
1	C13	Capacitor, MLCC, 390 pF, 0603	Vishay	VJ0603Y391KXXA
1	R1	Resistor, 17.4 kΩ, 1%, 0603, SMD	Vishay or equivalent	CRCW06031742F
1	R2	Resistor, 5.6 kΩ, 1%, 0603, SMD	Vishay or equivalent	CRCW06035601F
1	R4	Resistor, 15 kΩ, 1%, 0603, SMD	Vishay or equivalent	CRCW06031502F
1	R6	Resistor, 150 Ω, 1%, 0603, SMD	Vishay or equivalent	CRCW060315R1F
1	R5	Resistor, 36 kΩ, 1%, 0603, SMD	Vishay or equivalent	CRCW06033162F
2	R13, R14	Resistor, 100 kΩ, 1%, 0603, SMD	Vishay or equivalent	CRCW06031003F
2	R7, R12	Resistor, 2 Ω, 1%, 0603, SMD	Vishay or equivalent	CRCW06032R00F
3	R8, RA10, RB9	Resistor, 0 Ω, 1%, 0603, SMD	Vishay or equivalent	CRCW06030R00F
1	R11	Resistor, 0 Ω, 1%, 1206, SMD	Vishay or equivalent	CRCW12060R00F
1	R3	OPEN	Vishay or equivalent	
1	RA9	OPEN	Vishay or equivalent	
1	RB10	OPEN	Vishay or equivalent	
2	C11, C14	OPEN		
2	V_{OUT}, GND	Terminal		

ORDERING GUIDE

Model	Description
ADP1621-EVAL	Evaluation Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

NOTES

EB06358-0-11/06(0)