

# PMN49EN

N-channel TrenchMOS logic level FET

Rev. 01 — 13 April 2007

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

### 1.2 Features

- Logic level threshold
- Fast switching

### 1.3 Applications

- Battery management
- High-speed switching

### 1.4 Quick reference data

- $V_{DS} \leq 30\text{ V}$
- $I_D \leq 4.6\text{ A}$
- $R_{DS(on)} \leq 47\text{ m}\Omega$
- $Q_{GD} = 1.6\text{ nC (typ)}$

## 2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1, 2, 5, 6	drain (D)	<p>SOT457 (TSOP6)</p>	<p>mbb076 S</p>
3	gate (G)		
4	source (S)		

### 3. Ordering information

**Table 2. Ordering information**

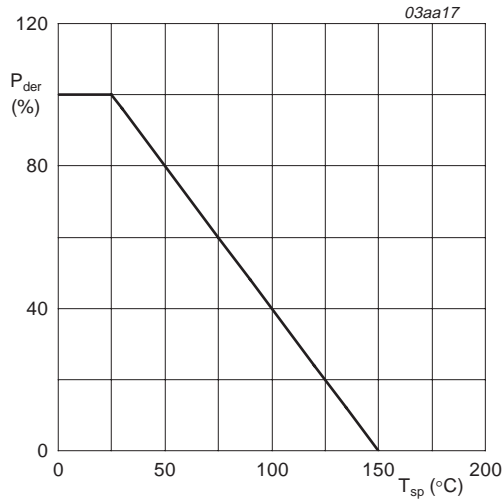
Type number	Package		Version
	Name	Description	
PMN49EN	SC-74	plastic surface-mounted package (TSOP6); 6 leads	SOT457

### 4. Limiting values

**Table 3. Limiting values**

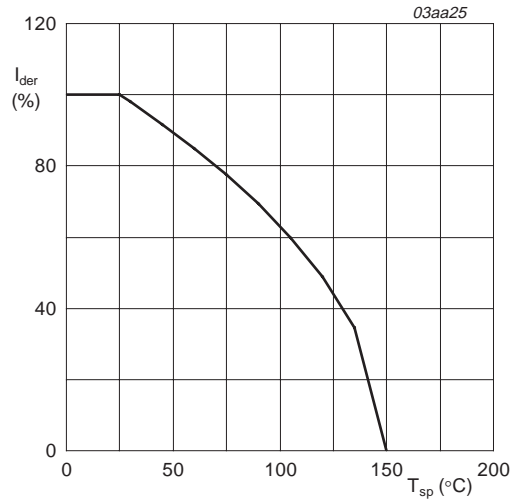
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	30	V
$V_{DGR}$	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	30	V
$V_{GS}$	gate-source voltage		-	$\pm 20$	V
$I_D$	drain current	$T_{sp} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 2</a> and <a href="#">3</a>	-	4.6	A
		$T_{sp} = 100\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 2</a>	-	2.9	A
$I_{DM}$	peak drain current	$T_{sp} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; see <a href="#">Figure 3</a>	-	18.4	A
$P_{tot}$	total power dissipation	$T_{sp} = 25\text{ °C}$ ; see <a href="#">Figure 1</a>	-	1.75	W
$T_{stg}$	storage temperature		-55	+150	°C
$T_j$	junction temperature		-55	+150	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{sp} = 25\text{ °C}$	-	1.4	A
$I_{SM}$	peak source current	$T_{sp} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	5.6	A



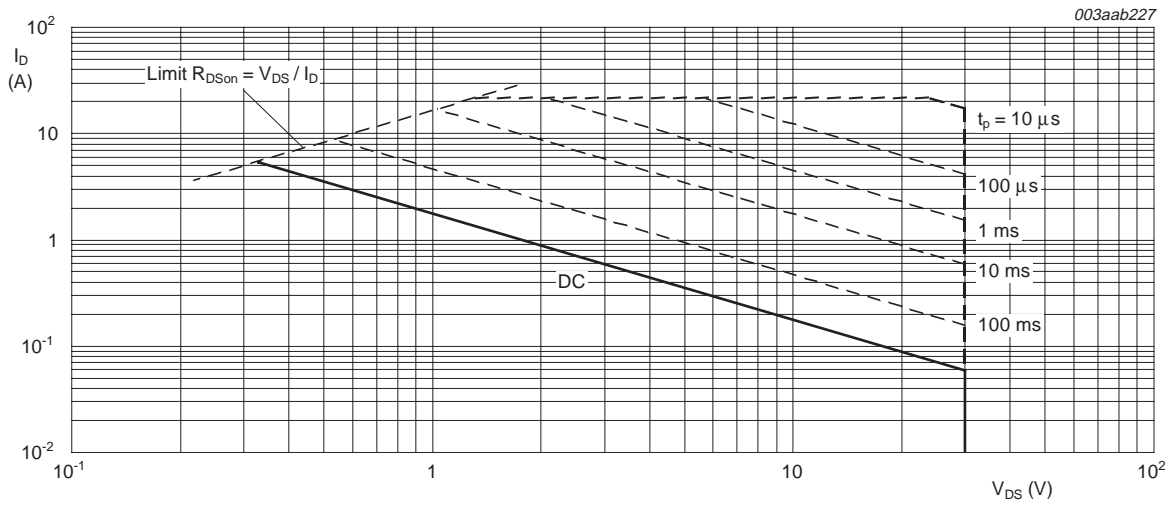
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature



T<sub>sp</sub> = 25 °C; I<sub>DM</sub> is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

### 5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see <a href="#">Figure 4</a>	-	-	70	K/W

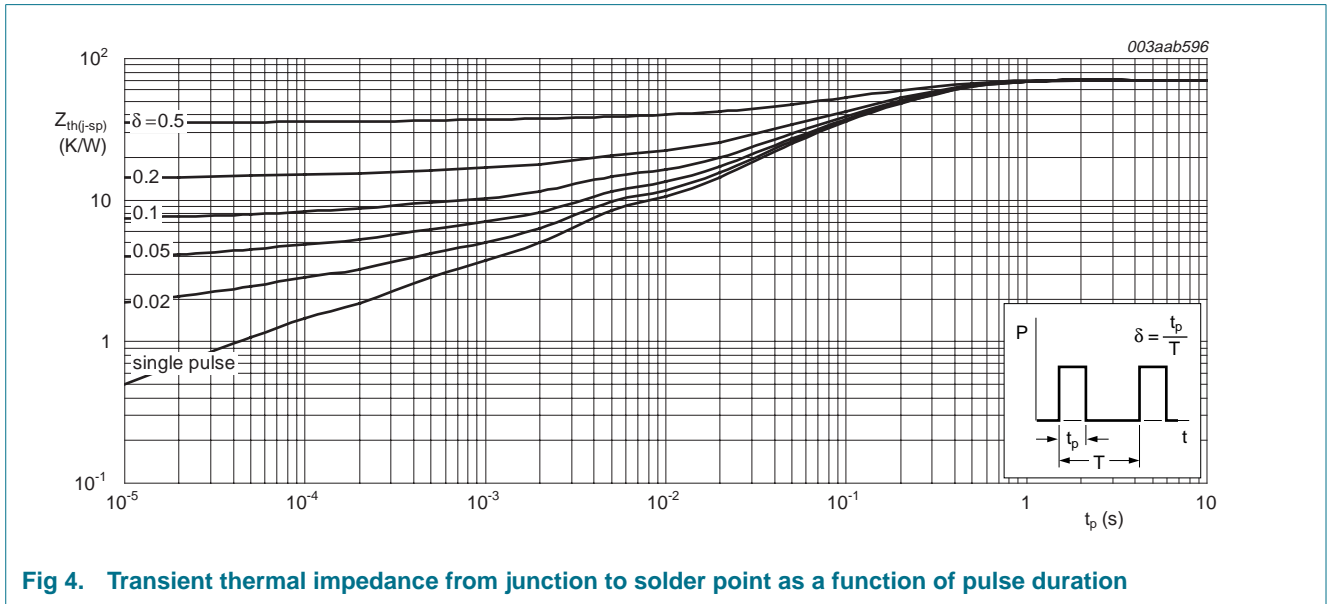


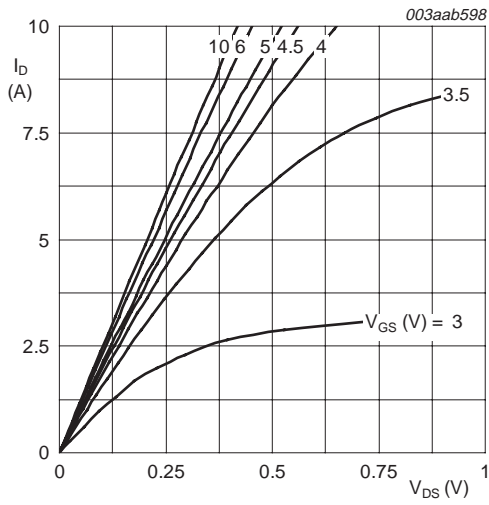
Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

## 6. Characteristics

**Table 5. Characteristics**

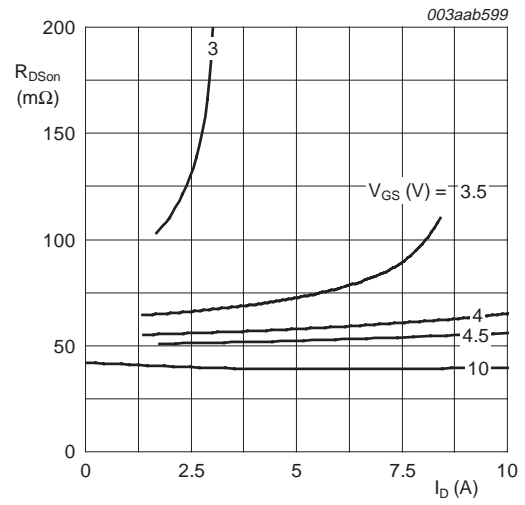
$T_j = 25\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}; V_{GS} = 0\ \text{V}$				
		$T_j = 25\text{ °C}$	30	-	-	V
		$T_j = -55\text{ °C}$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}; V_{DS} = V_{GS}$ ; see <a href="#">Figure 9</a> and <a href="#">10</a>				
		$T_j = 25\text{ °C}$	1	1.5	2	V
		$T_j = 150\text{ °C}$	0.6	-	-	V
		$T_j = -55\text{ °C}$	-	-	2.2	V
$I_{DSS}$	drain leakage current	$V_{DS} = 30\ \text{V}; V_{GS} = 0\ \text{V}$				
		$T_j = 25\text{ °C}$	-	-	1	$\mu\text{A}$
		$T_j = 150\text{ °C}$	-	-	100	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = \pm 20\ \text{V}; V_{DS} = 0\ \text{V}$	-	10	100	nA
$R_G$	gate resistance	$f = 1\ \text{MHz}; V_{GS(AC)} = 150\ \text{mV}$	-	1.9	-	$\Omega$
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\ \text{V}; I_D = 2\ \text{A}$ ; see <a href="#">Figure 6</a> and <a href="#">8</a>				
		$T_j = 25\text{ °C}$	-	40	47	m $\Omega$
		$T_j = 150\text{ °C}$	-	68	80	m $\Omega$
		$V_{GS} = 4.5\ \text{V}; I_D = 1.5\ \text{A}$ ; see <a href="#">Figure 6</a> and <a href="#">8</a>	-	49	60	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 3\ \text{A}; V_{DS} = 15\ \text{V}; V_{GS} = 4.5\ \text{V}$ ; see <a href="#">Figure 11</a> and <a href="#">12</a>	-	8.8	-	nC
$Q_{GS}$	gate-source charge		-	1.1	-	nC
$Q_{GD}$	gate-drain charge		-	1.6	-	nC
$V_{GS(pl)}$	gate-source plateau voltage		-	2.83	-	V
$C_{iss}$	input capacitance	$V_{GS} = 0\ \text{V}; V_{DS} = 30\ \text{V}; f = 1\ \text{MHz}$ ; see <a href="#">Figure 14</a>	-	350	-	pF
$C_{oss}$	output capacitance		-	100	-	pF
$C_{rss}$	reverse transfer capacitance		-	64.1	-	pF
$C_{iss}$	input capacitance	$V_{GS} = 0\ \text{V}; V_{DS} = 0\ \text{V}; f = 1\ \text{MHz}$	-	570	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15\ \text{V}; R_L = 15\ \Omega; V_{GS} = 10\ \text{V}; R_G = 6\ \Omega$	-	4.1	-	ns
$t_r$	rise time		-	4.3	-	ns
$t_{d(off)}$	turn-off delay time		-	12.9	-	ns
$t_f$	fall time		-	4.9	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 1.5\ \text{A}; V_{GS} = 0\ \text{V}$ ; see <a href="#">Figure 13</a>	-	0.79	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 2\ \text{A}; di_S/dt = -100\ \text{A}/\mu\text{s}; V_{GS} = 0\ \text{V}$	-	19.25	-	ns
$Q_r$	recovered charge		-	0.73	-	nC



$T_j = 25^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



$T_j = 25^\circ\text{C}$

Fig 6. Drain-source on-state resistance as a function of drain current; typical values

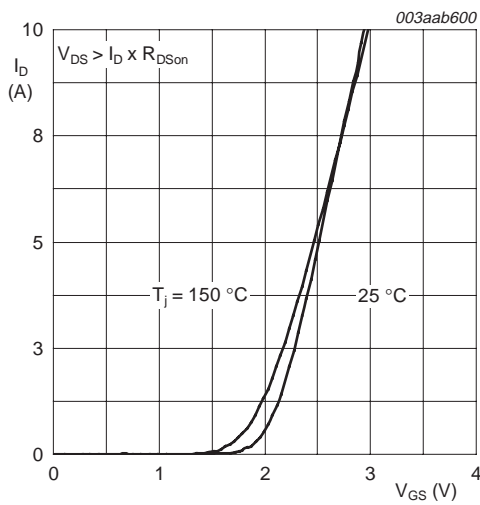
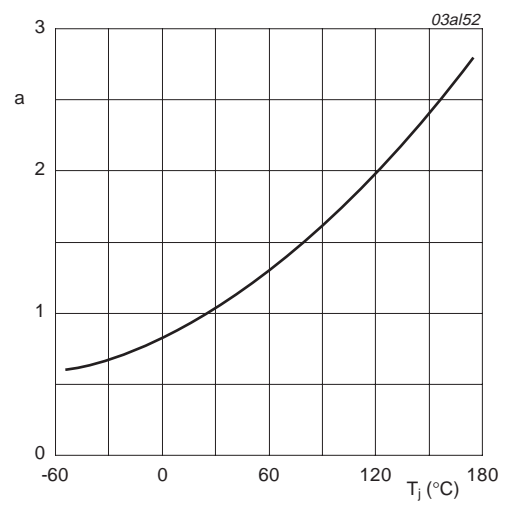
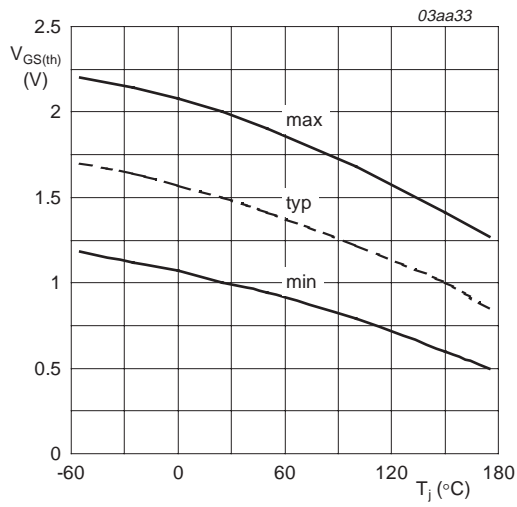


Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



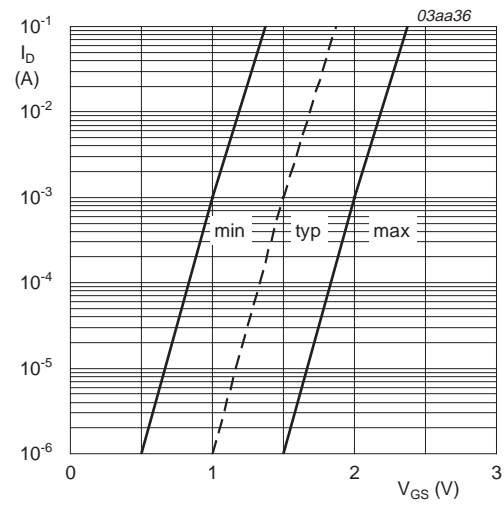
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



$T_j = 25 \text{ }^{\circ}C; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage

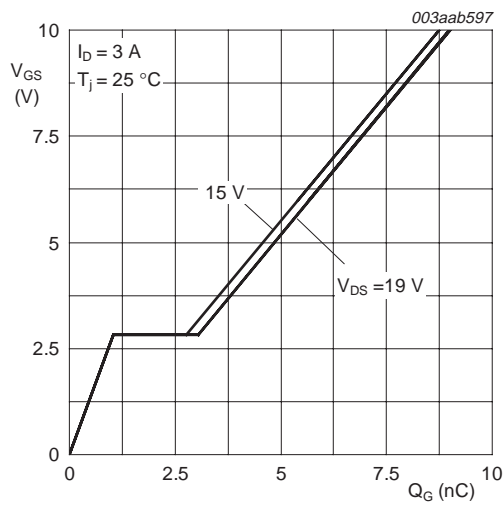


Fig 11. Gate-source voltage as a function of gate charge; typical values

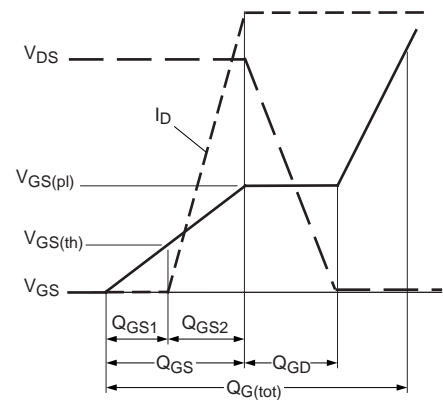
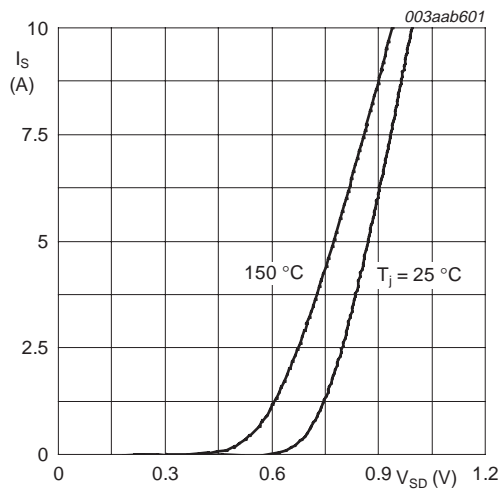
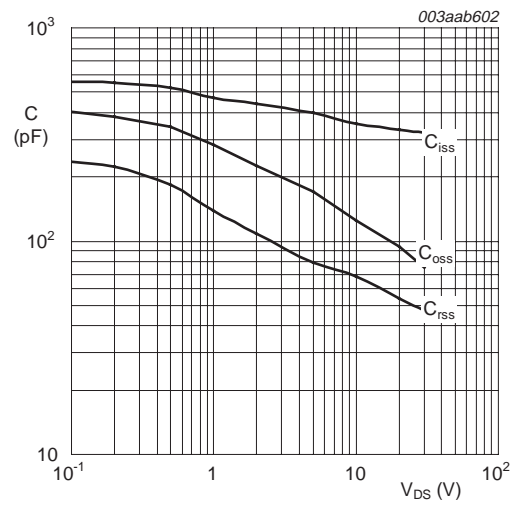


Fig 12. Gate charge waveform definitions



$T_J = 25\text{ }^\circ\text{C}$  and  $150\text{ }^\circ\text{C}$ ;  $V_{GS} = 0\text{ V}$

**Fig 13. Source current as a function of source-drain voltage; typical values**



$V_{GS} = 0\text{ V}$ ;  $f = 1\text{ MHz}$

**Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



7. Package outline

Plastic surface-mounted package (TSOP6); 6 leads

SOT457

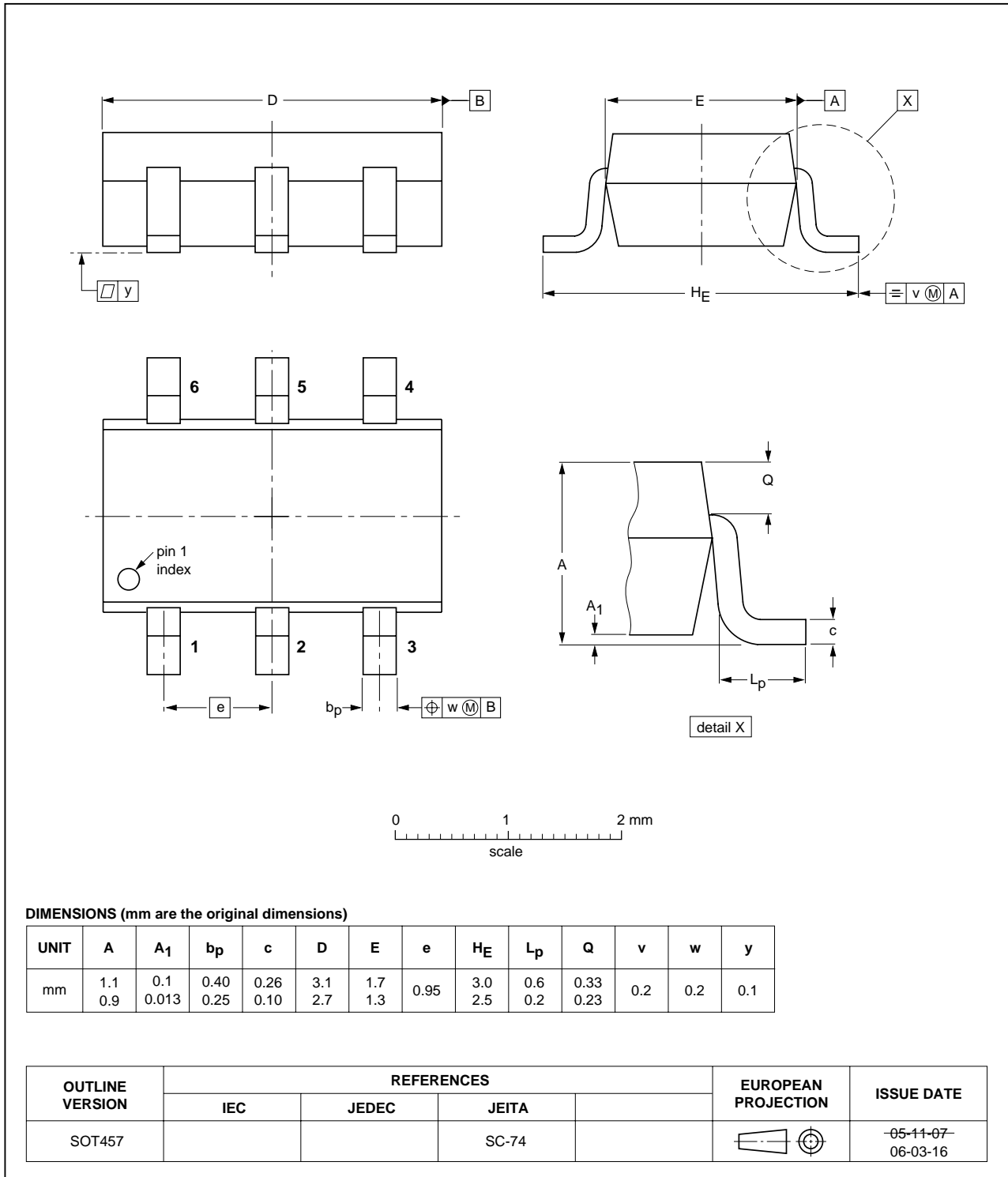


Fig 15. Package outline SOT457 (TSOP6)

## 8. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMN49EN_1	20070413	Product data sheet	-	-

## 9. Legal information

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Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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## 11. Contents

<b>1</b>	<b>Product profile</b> . . . . .	<b>1</b>
1.1	General description . . . . .	1
1.2	Features . . . . .	1
1.3	Applications . . . . .	1
1.4	Quick reference data . . . . .	1
<b>2</b>	<b>Pinning information</b> . . . . .	<b>1</b>
<b>3</b>	<b>Ordering information</b> . . . . .	<b>2</b>
<b>4</b>	<b>Limiting values</b> . . . . .	<b>2</b>
<b>5</b>	<b>Thermal characteristics</b> . . . . .	<b>4</b>
<b>6</b>	<b>Characteristics</b> . . . . .	<b>5</b>
<b>7</b>	<b>Package outline</b> . . . . .	<b>9</b>
<b>8</b>	<b>Revision history</b> . . . . .	<b>10</b>
<b>9</b>	<b>Legal information</b> . . . . .	<b>11</b>
9.1	Data sheet status . . . . .	11
9.2	Definitions . . . . .	11
9.3	Disclaimers . . . . .	11
9.4	Trademarks . . . . .	11
<b>10</b>	<b>Contact information</b> . . . . .	<b>11</b>
<b>11</b>	<b>Contents</b> . . . . .	<b>12</b>

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