Ordering number : ENA2226B

LC75843UGA

CMOS IC

1/1 to 1/4 Duty General-Purpose LCD Display Driver

ON Semiconductor®

http://onsemi.com

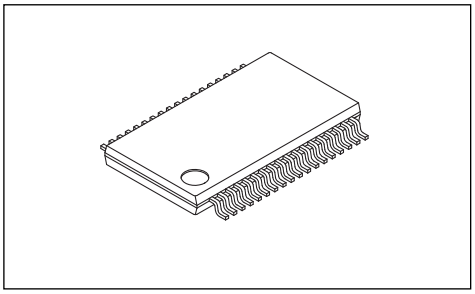
Overview

The LC75843UGA is the 1/1 to 1/4 duty general-purpose microprocessor-controlled LCD driver that can be used in applications such as Automotive display. In addition to being able to drive up to 100 segments directly, the LC75843UGA can also control up to 4 general-purpose output ports. Because it has the PWM output of a maximum of 3ch, the brightness control of the LED backlight of RGB can be done. Incorporation of an oscillation circuit helps to reduce the number of external resistors and capacitors required.

Features

- Support for static(1/1duty) or 1/2-duty 1/2-bias or 1/3-duty 1/3-bias or 1/4-duty 1/3-bias drive techniques under serial data control.
  - When 1/1-duty : Capable of driving up to 28 segments
  - When 1/2-duty : Capable of driving up to 54 segments
  - When 1/3-duty : Capable of driving up to 78 segments
  - When 1/4-duty : Capable of driving up to 100 segments
- Serial data input supports CCB format communication with the system controller. (Support 3.3V and 5V operation)
- Serial data control of the power-saving mode based backup function and the all segments forced off function.
- Serial data control of switching between the segment output port and general-purpose output port function. (Support for up to 4 general-purpose output ports)
- Support for the PWM output function of a maximum of 3ch. (It can output from the general-purpose output port).
- Support for clock output function of 1ch.(It can output from the general-purpose output port).
- Serial data control of the frame frequency of the common and segment output waveforms.
- Serial data control of switching between the internal oscillator operating mode and external clock operating mode.
- High generality, since display data is displayed directly without the intervention of a decoder circuit.
- Built-in LCD drive bias voltage stabilization circuit.
- The INH pin allows the display to be forced to the off state.
- Incorporation of an oscillator circuit. (Incorporation of resistor and capacitor for an oscillation)
- AEC-Q100 qualified and PPAP capable.

- CCB is ON Semiconductor® 's original format. All addresses are managed by ON Semiconductor® for this format.



TSSOP36(275mil)

- CCB is a registered trademark of Semiconductor Components Industries, LLC.

ORDERING INFORMATION

See detailed ordering and shipping information on page 35 of this data sheet.

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	-0.3 to +6.8	V
Input voltage	V_{IN}	CE, CL, DI, $\overline{INH}$, OSCI	-0.3 to +6.8	V
Output voltage	V_{OUT}	S1 to S28, COM1 to COM4, P1 to P4	-0.3 to V_{DD}+0.3	V
Output current	$I_{OUT}1$	S1 to S28	300	μA
	$I_{OUT}2$	COM1 to COM4	3	mA
	$I_{OUT}3$	P1 to P4	5	
Allowable power dissipation	Pd max	Ta = 105°C	50	mW
Operating temperature	Topr		-40 to +105	°C
Storage temperature	Tstg		-55 to +125	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable Operating Ranges at Ta = -40 to +105°C, V_{SS} = 0V

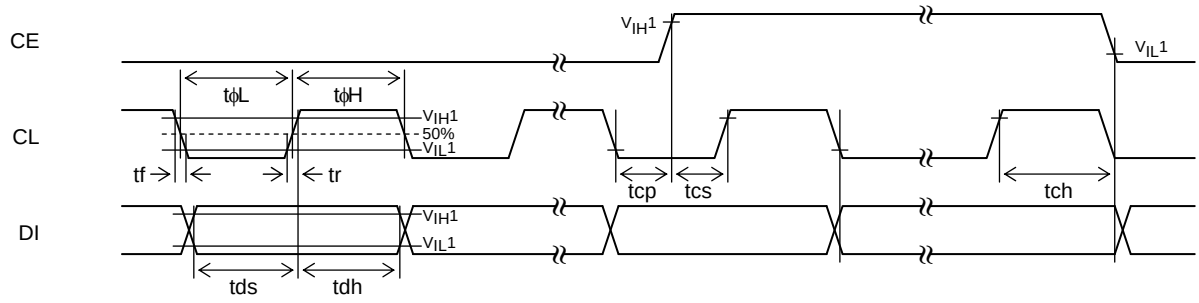
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	4.5		6.3	V
Input high level voltage	$V_{IH}1$	CE, CL, DI, $\overline{INH}$	0.4V_{DD}		6.3	V
	$V_{IH}2$	OSCI	0.4V_{DD}		6.3	
Input low level voltage	$V_{IL}1$	CE, CL, DI, $\overline{INH}$	0		0.2V_{DD}	V
	$V_{IL}2$	OSCI	0		0.2V_{DD}	
External clock operating frequency	f_{CK}	OSCI, External clock operating mode [Figure 3]	10	300	600	kHz
External clock duty cycle	D_{CK}	OSCI, External clock operating mode [Figure 3]	30	50	70	%
Data setup time	tds	CL, DI [Figure 1], [Figure 2]	160			ns
Data hold time	tdh	CL, DI [Figure 1], [Figure 2]	160			ns
CE wait time	tcp	CE, CL [Figure 1], [Figure 2]	160			ns
CE setup time	tcs	CE, CL [Figure 1], [Figure 2]	160			ns
CE hold time	tch	CE, CL [Figure 1], [Figure 2]	160			ns
High level clock pulse width	tϕH	CL [Figure 1], [Figure 2]	160			ns
Low level clock pulse width	tϕL	CL [Figure 1], [Figure 2]	160			ns
Rise time	tr	CE, CL, DI [Figure 1], [Figure 2]		160		ns
Fall time	tf	CE, CL, DI [Figure 1], [Figure 2]		160		ns
$\overline{INH}$ switching time	tc	$\overline{INH}$, CE [Figure 4], [Figure 5] [Figure 6], [Figure 7]	10			μs

Electrical Characteristics for the Allowable Operating Ranges

Parameter	Symbol	Pin	Conditions	Ratings			Unit
				min	typ	max	
Hysteresis	V_H	CE, CL, DI, $\overline{INH}$			$0.03V_{DD}$		V
Input high level current	$I_{IH}1$	CE, CL, DI, $\overline{INH}$	V_I = 6.3V			5.0	μA
	$I_{IH}2$	OSCI	V_I = 6.3V			5.0	
Input low level current	$I_{IL}1$	CE, CL, DI, $\overline{INH}$	V_I = 0V	-5.0			μA
	$I_{IL}2$	OSCI	V_I = 0V	-5.0			
Output high level voltage	$V_{OH}1$	S1 to S28	I_O = -20μA	V_{DD}-0.9			V
	$V_{OH}2$	COM1 to COM4	I_O = -100μA	V_{DD}-0.9			
	$V_{OH}3$	P1 to P4	I_O = -1mA	V_{DD}-0.9			
Output low level voltage	$V_{OL}1$	S1 to S28	I_O = 20μA			0.9	V
	$V_{OL}2$	COM1 to COM4	I_O = 100μA			0.9	
	$V_{OL}3$	P1 to P4	I_O = 1mA			0.9	
Output middle level voltage	$V_{MID}1$	S1 to S25, S28	1/3 bias I_O = ±20μA	$2/3V_{DD}$ -0.9		$2/3V_{DD}$ +0.9	V
	$V_{MID}2$	S1 to S25, S28	1/3 bias I_O = ±20μA	$1/3V_{DD}$ -0.9		$1/3V_{DD}$ +0.9	
	$V_{MID}3$	COM1 to COM4	1/3 bias I_O = ±100μA	$2/3V_{DD}$ -0.9		$2/3V_{DD}$ +0.9	
	$V_{MID}4$	COM1 to COM4	1/3 bias I_O = ±100μA	$1/3V_{DD}$ -0.9		$1/3V_{DD}$ +0.9	
	$V_{MID}5$	COM1, COM2	1/2 bias I_O = ±100μA	$1/2V_{DD}$ -0.9		$1/2V_{DD}$ +0.9	
Oscillator frequency	fosc	Internal oscillator circuit	Internal oscillator operating mode	240	300	360	kHz
Current drain	$I_{DD}1$	V_{DD}	Power-saving mode			100	μA
	$I_{DD}2$	V_{DD}	V_{DD} = 6.3V Output open Internal oscillator operating mode		750	1500	
	$I_{DD}3$	V_{DD}	V_{DD} = 6.3V Output open External clock operating mode f_{CK} = 300kHz $V_{IH}2 = 0.5V_{DD}$ $V_{IL}2 = 0.1V_{DD}$		750	1500	

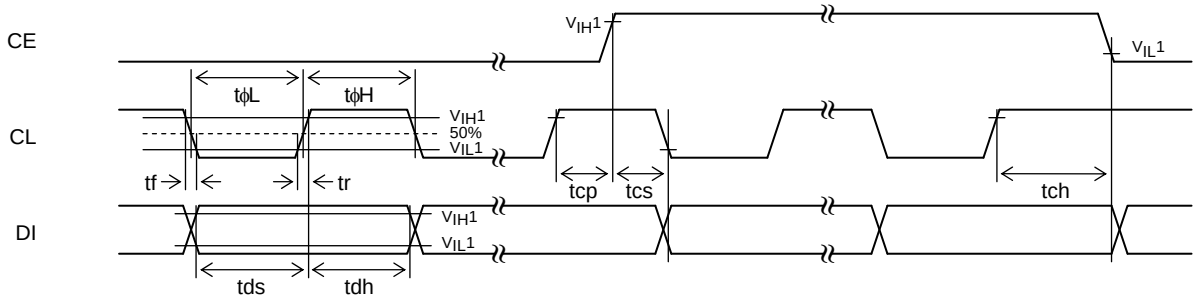
*We have a case to change these electrical characteristics without a notice for improvement.

1. When CL is stopped at the low level



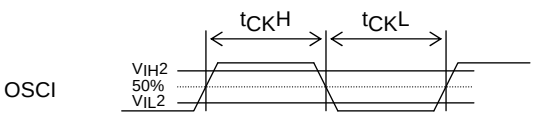
[Figure 1]

2. When CL is stopped at the high level



[Figure 2]

3. OSCI pin clock timing in external clock operating mode

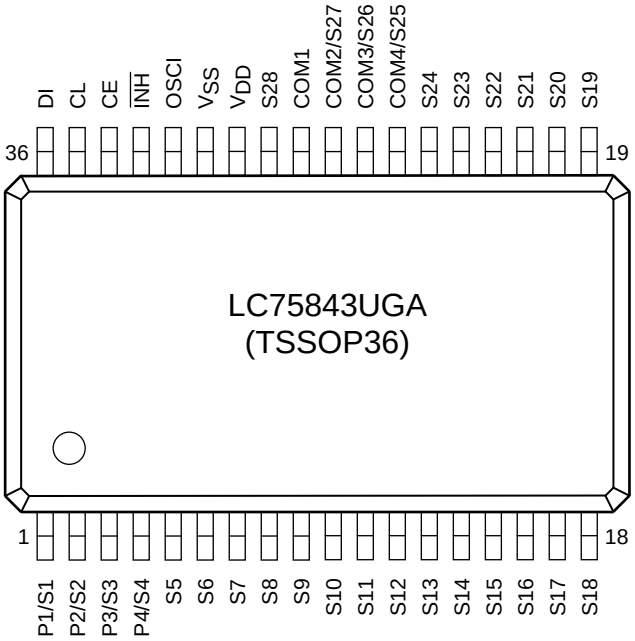


$$f_{CK} = \frac{1}{t_{CK}H + t_{CK}L} \quad [kHz]$$

$$D_{CK} = \frac{t_{CK}H}{t_{CK}H + t_{CK}L} \times 100[\%]$$

[Figure 3]

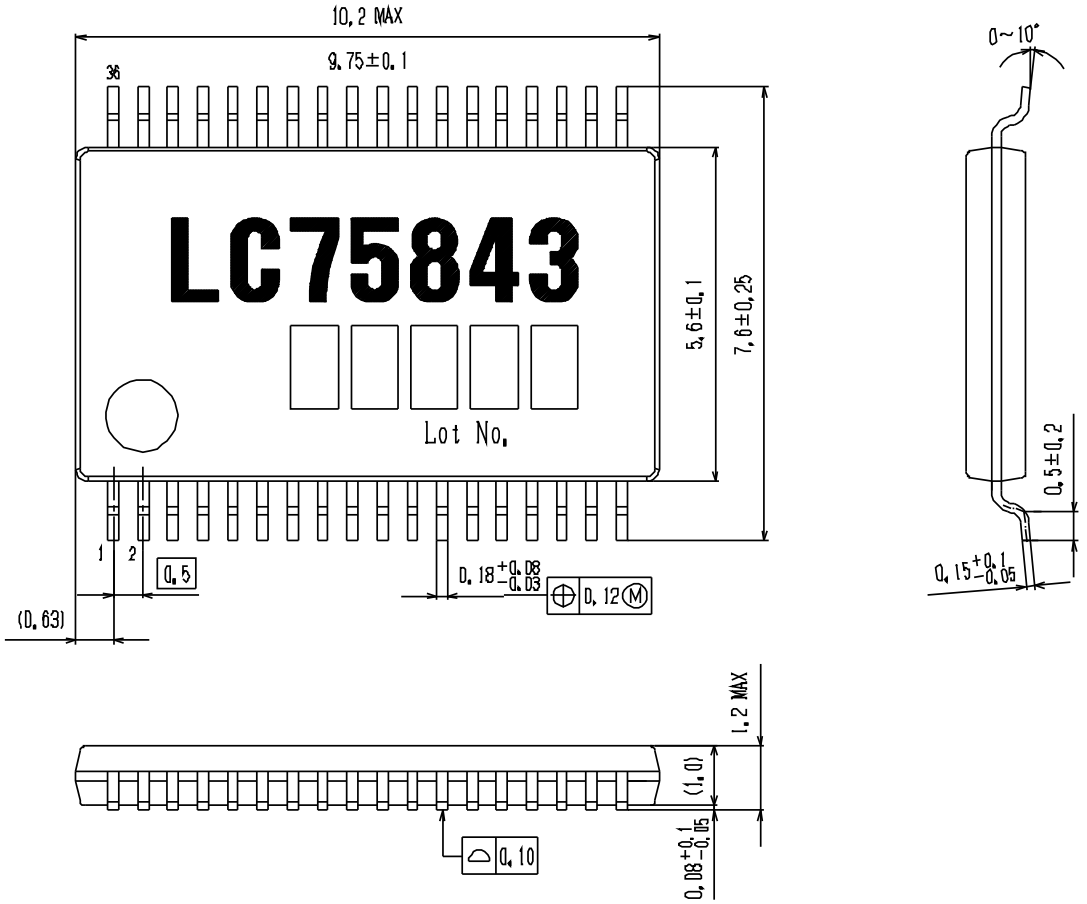
Pin Assignment



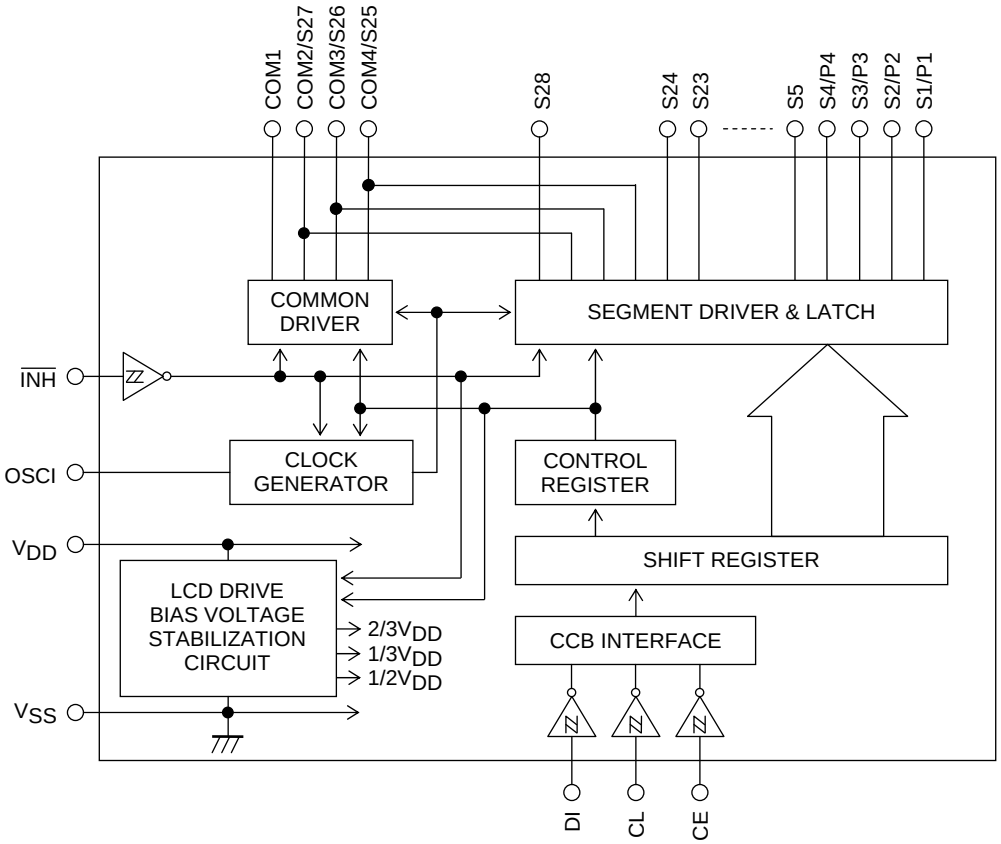
Top view

Package Dimensions

TSSOP36(275mil)
unit : mm



Block Diagram



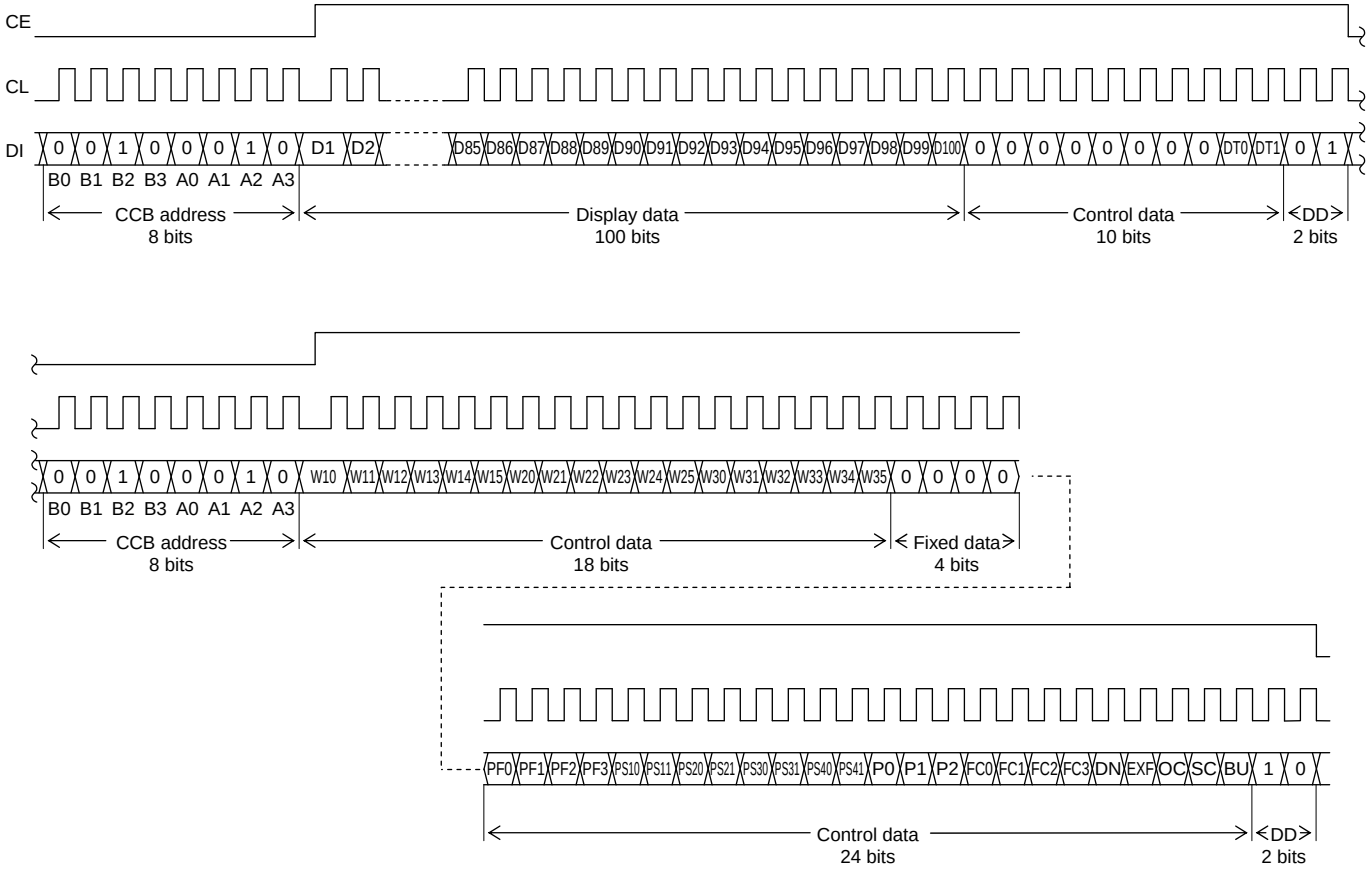
Pin Functions

Symbol	Pin No.	Function	Active	I/O	Handling when unused
S1/P1 to S4/P4 S5 to S24 S28	1 to 4 5 to 24 29	Segment outputs for displaying the display data transferred by serial data input. The S1/P1 to S4/P4 pins can be used as general-purpose output ports under serial data control.	-	O	OPEN
COM1 COM2/S27 COM3/S26 COM4/S25	28 27 26 25	Common driver outputs The frame frequency is fo[Hz]. The COM2/S27 to COM4/S25 pin can be used as a segment output by control data.	-	O	OPEN
OSCI	32	This is input pin for the external clock. Input the clock at external clock operating mode. Furthermore, connect to GND at internal oscillator operating mode.	-	I	GND
CE CL DI	34 35 36	Serial data transfer inputs. Must be connected to the controller. CE : Chip enable CL : Synchronization clock DI : Transfer data	H ↑ -	I I I	GND
$\overline{INH}$	33	Display off control input •$\overline{INH}$=low(V_{SS})….Display forced off S1/P1 to S4/P4=low (V_{SS}) (These pins are forcibly set to the general-purpose output port function and held at the V_{SS} level.) S5 to S24, S28=low(V_{SS}) COM1=low(V_{SS}) COM2/S27 to COM4/S25=low(V_{SS}) Stops the internal oscillator. Inhibits external clock input. •$\overline{INH}$=high(V_{DD})…Display on Enables the internal oscillator circuit. (Internal oscillator operating mode) Enables external clock input. (External clock operating mode) However, serial data transfer is possible when the display is forced off.	L	I	GND
V_{DD}	30	Power supply pin. A power voltage of 4.5 to 6.3V must be applied to this pin.	-	-	-
V_{SS}	31	Ground pin. Must be connected to ground.	-	-	-

Serial Data Input

1. 1/4 duty

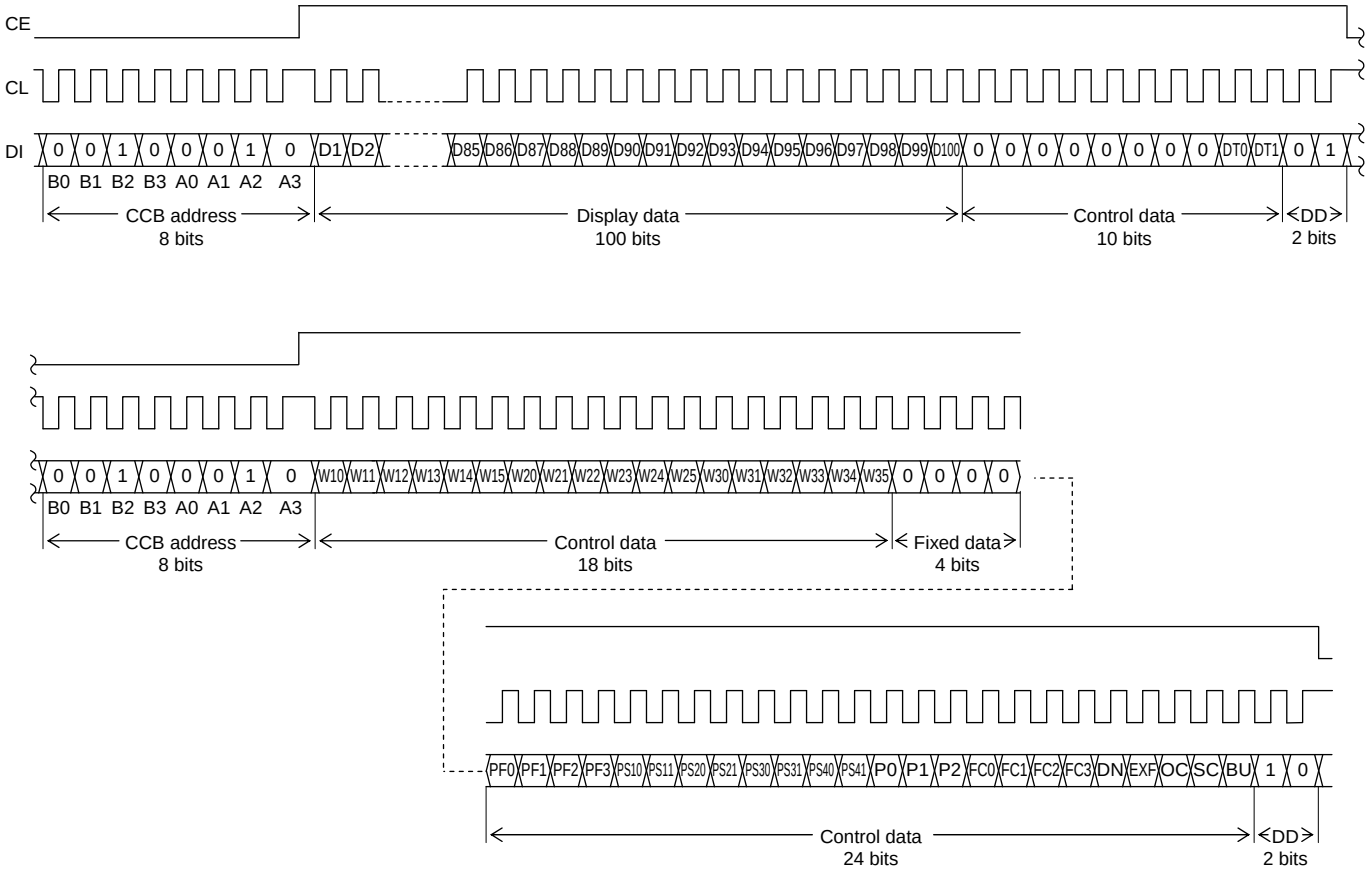
(1) When CL is stopped at the low level



Note: DD is the direction data

- CCB address ..... "44H"
- D1 to D100 ..... Display data
- DT0, DT1 ..... 1/1-duty to 1/4-duty drive switching control data
- W 10 to W15, W20 to W25, W30 to W35 ... PWM data of the PWM output
- PF0 to PF3 ..... PWM output waveform frame frequency setting control data
- PS10, PS11 to PS40, PS41 ..... General-purpose output port (P1 to P4) function setting control data
- P0 to P2 ..... Segment output port/general-purpose output port switching control data
- FC0 to FC3 ..... Common/segment output waveform frame frequency setting control data
- DN ..... S28 pin state setting control data
- EXF ..... External clock operating frequency setting control data
- OC ..... Internal oscillator operating mode/external clock operating mode switching control data
- SC ..... Segment on/off control data
- BU ..... Normal mode/power-saving mode control data

(2) When CL is stopped at the high level



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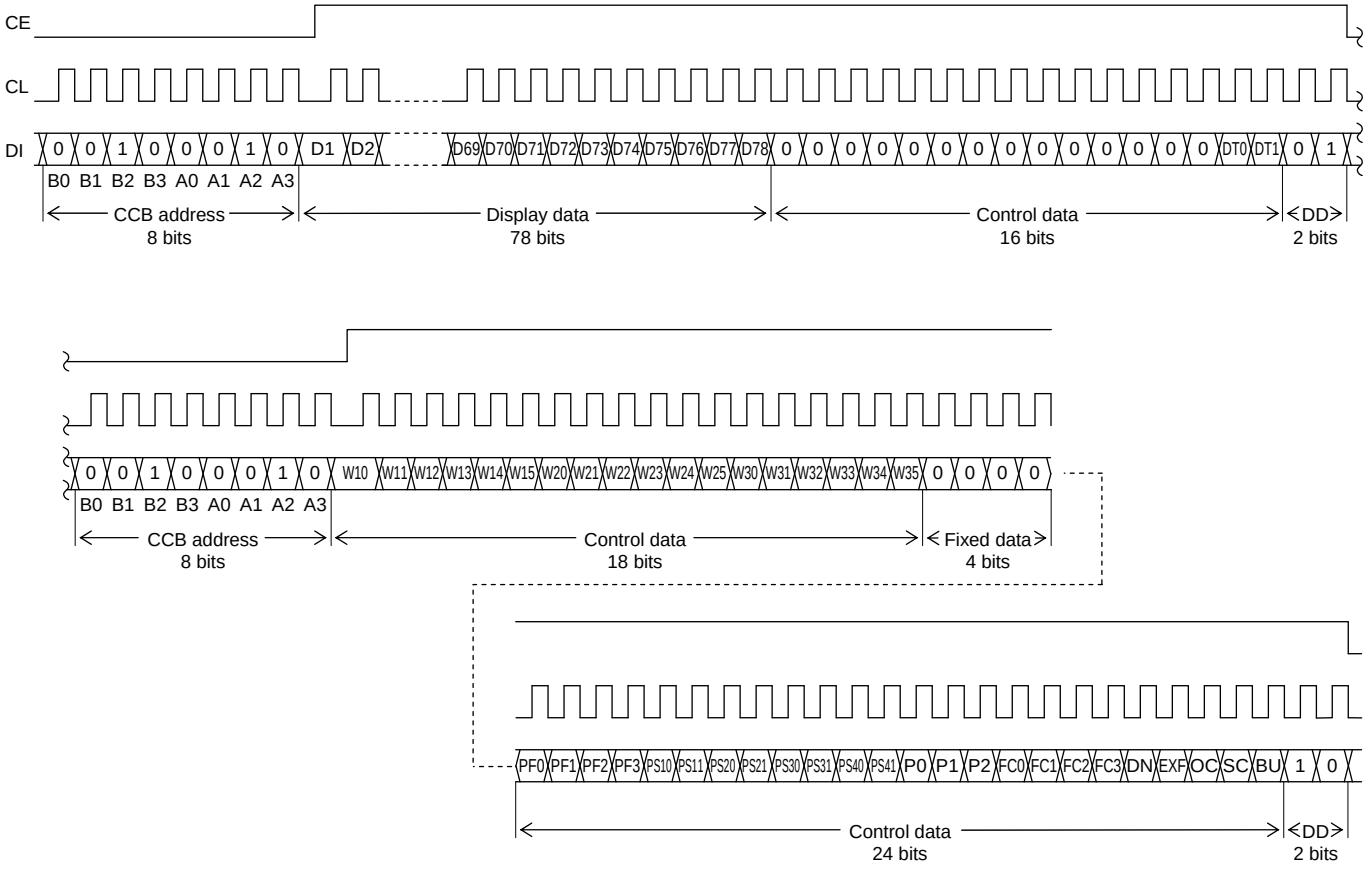
- CCB address ..... "44H"
- D1 to D100 ..... Display data
- DT0, DT1 ..... 1/1-duty to 1/4-duty drive switching control data
- W 10 to W15, W20 to W25, W30 to W35 ... PWM data of the PWM output
- PF0 to PF3 ..... PWM output waveform frame frequency setting control data
- PS10, PS11 to PS40, PS41 ..... General-purpose output port (P1 to P4) function setting control data
- P0 to P2 ..... Segment output port/general-purpose output port switching control data
- FC0 to FC3 ..... Common/segment output waveform frame frequency setting control data
- DN ..... S28 pin state setting control data
- EXF ..... External clock operating frequency setting control data
- OC ..... Internal oscillator operating mode/external clock operating mode switching control data
- SC ..... Segment on/off control data
- BU ..... Normal mode/power-saving mode control data

2. 1/3 duty

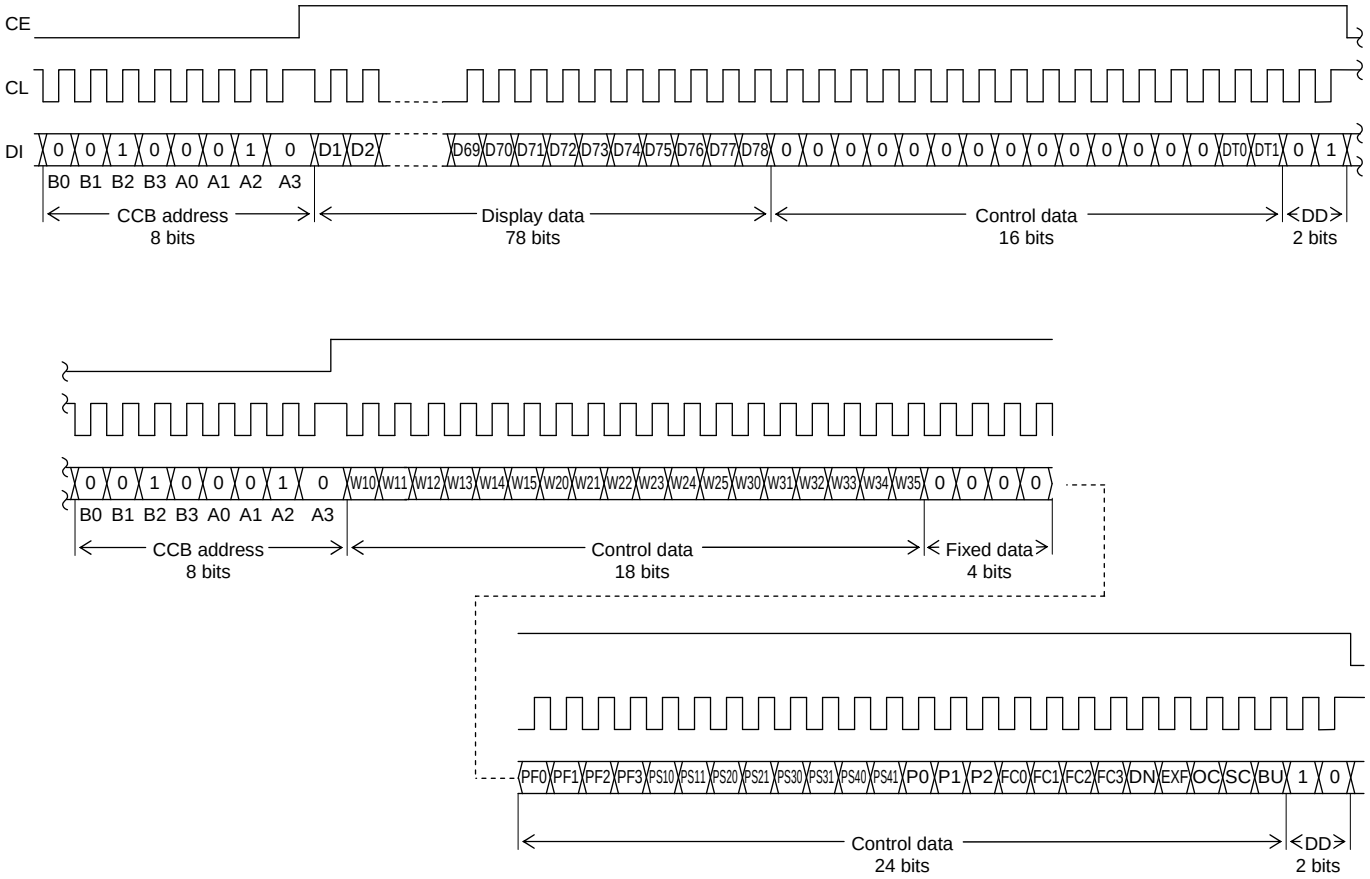
(1) When CL is stopped at the low level



Note: DD is the direction data

- CCB address ..... "44H"
- D1 to D78 ..... Display data
- DT0, DT1 ..... 1/1-duty to 1/4-duty drive switching control data
- W 10 to W15, W20 to W25, W30 to W35 ... PWM data of the PWM output
- PF0 to PF3 ..... PWM output waveform frame frequency setting control data
- PS10, PS11 to PS40, PS41 ..... General-purpose output port (P1 to P4) function setting control data
- P0 to P2 ..... Segment output port/general-purpose output port switching control data
- FC0 to FC3 ..... Common/segment output waveform frame frequency setting control data
- DN ..... S28 pin state setting control data
- EXF ..... External clock operating frequency setting control data
- OC ..... Internal oscillator operating mode/external clock operating mode switching control data
- SC ..... Segment on/off control data
- BU ..... Normal mode/power-saving mode control data

(2) When CL is stopped at the high level



Note: DD is the direction data

- CCB address ..... "44H"
- D1 to D78 ..... Display data
- DT0, DT1 ..... 1/1-duty to 1/4-duty drive switching control data
- W 10 to W15, W20 to W25, W30 to W35 ... PWM data of the PWM output
- PF0 to PF3 ..... PWM output waveform frame frequency setting control data
- PS10, PS11 to PS40, PS41 ..... General-purpose output port (P1 to P4) function setting control data
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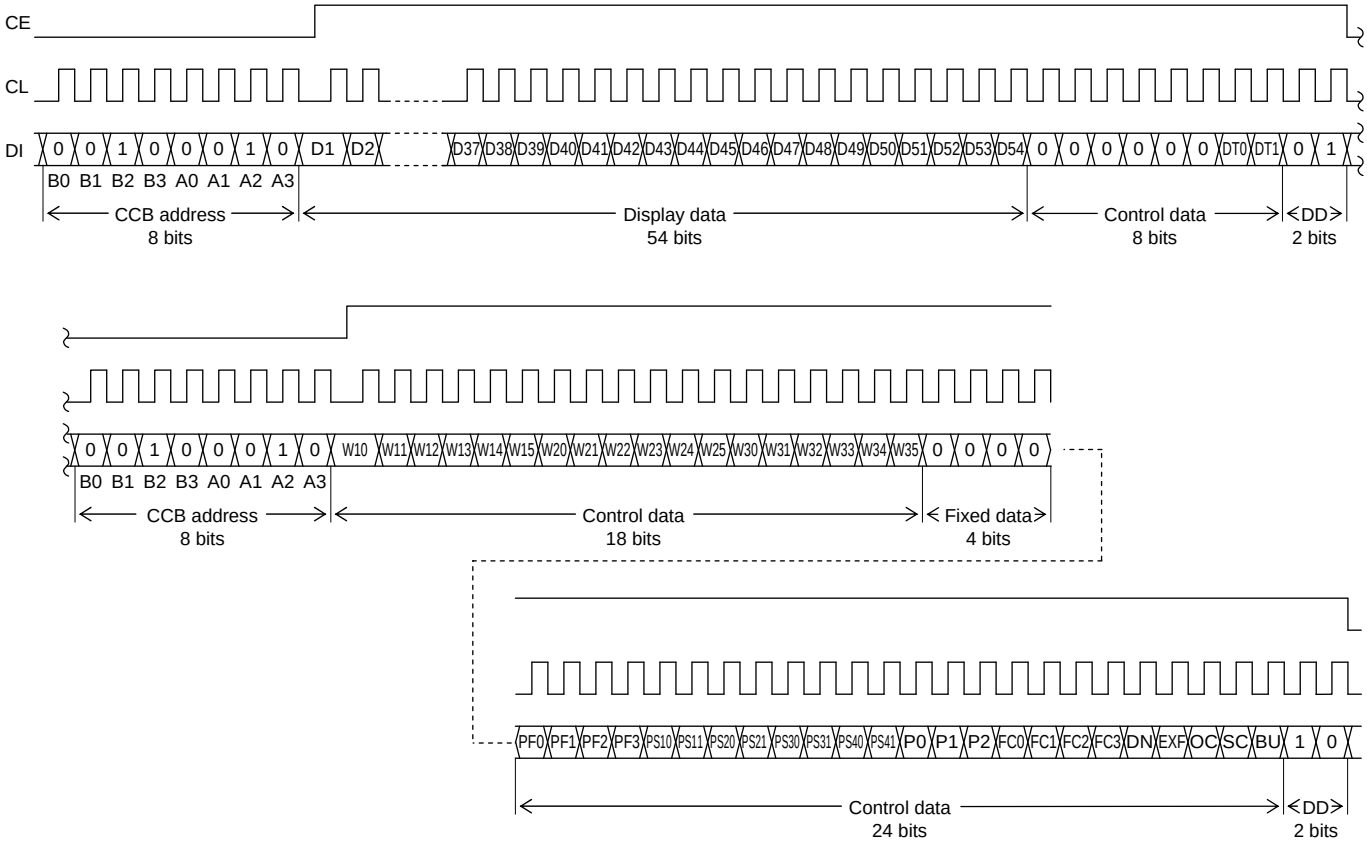
- EXF ..... External clock operating frequency setting control data
- OC ..... Internal oscillator operating mode/external clock operating mode switching control data
- SC ..... Segment on/off control data
- BU ..... Normal mode/power-saving mode control data

3. 1/2 duty

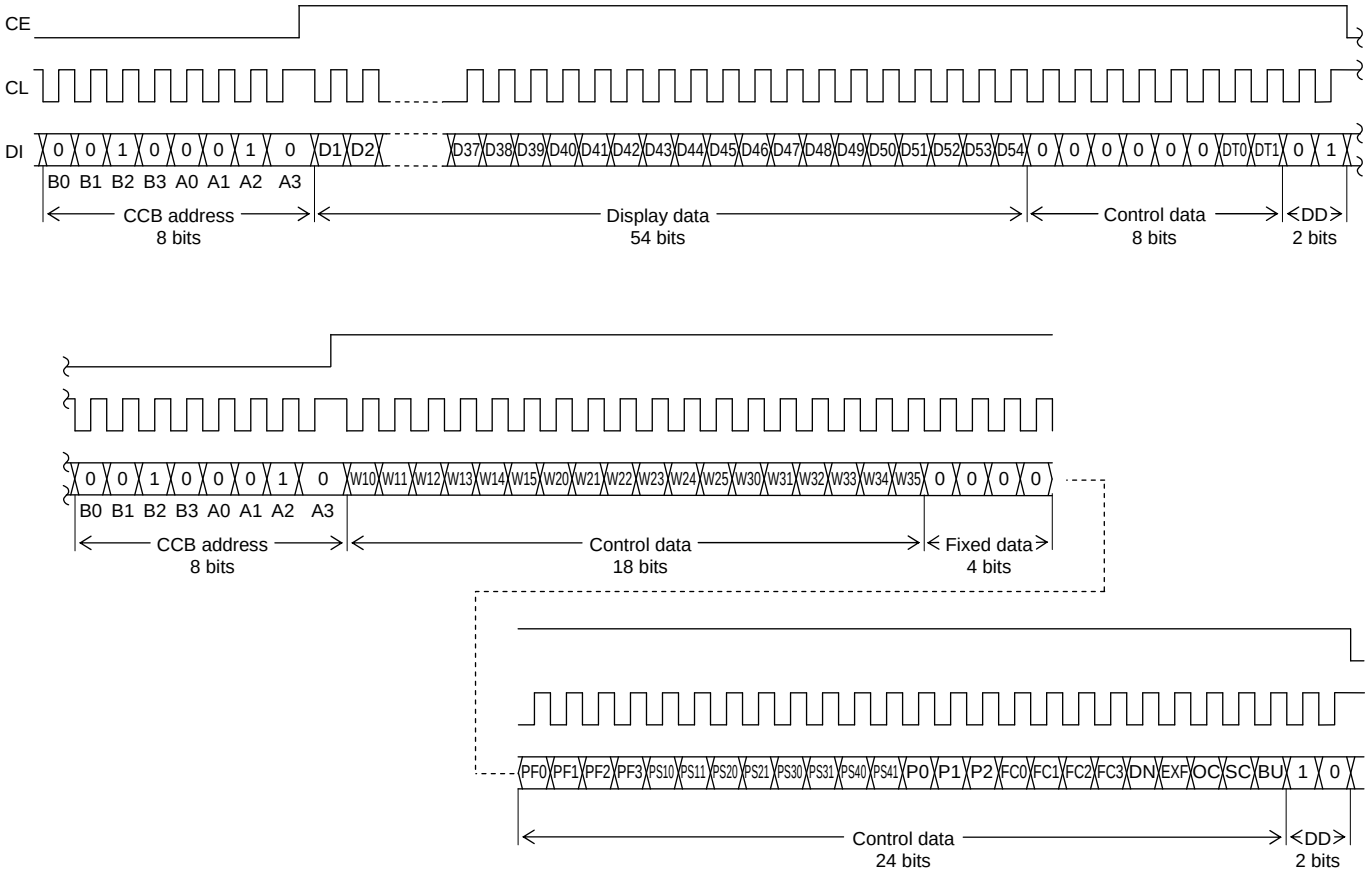
(1) When CL is stopped at the low level



Note: DD is the direction data

- CCB address ..... "44H"
- D1 to D54 ..... Display data
- DT0, DT1 ..... 1/1-duty to 1/4-duty drive switching control data
- W 10 to W15, W20 to W25, W30 to W35 ... PWM data of the PWM output
- PF0 to PF3 ..... PWM output waveform frame frequency setting control data
- PS10, PS11 to PS40, PS41 ..... General-purpose output port (P1 to P4) function setting control data
- P0 to P2 ..... Segment output port/general-purpose output port switching control data
- FC0 to FC3 ..... Common/segment output waveform frame frequency setting control data
- DN ..... S28 pin state setting control data
- EXF ..... External clock operating frequency setting control data
- OC ..... Internal oscillator operating mode/external clock operating mode switching control data
- SC ..... Segment on/off control data
- BU ..... Normal mode/power-saving mode control data

(2) When CL is stopped at the high level



Note: DD is the direction data

- CCB address ..... "44H"
- D1 to D54 ..... Display data
- DT0, DT1 ..... 1/1-duty to 1/4-duty drive switching control data
- W 10 to W15, W20 to W25, W30 to W35 ... PWM data of the PWM output
- PF0 to PF3 ..... PWM output waveform frame frequency setting control data
- PS10, PS11 to PS40, PS41 ..... General-purpose output port (P1 to P4) function setting control data
- P0 to P2 ..... Segment output port/general-purpose output port switching control data
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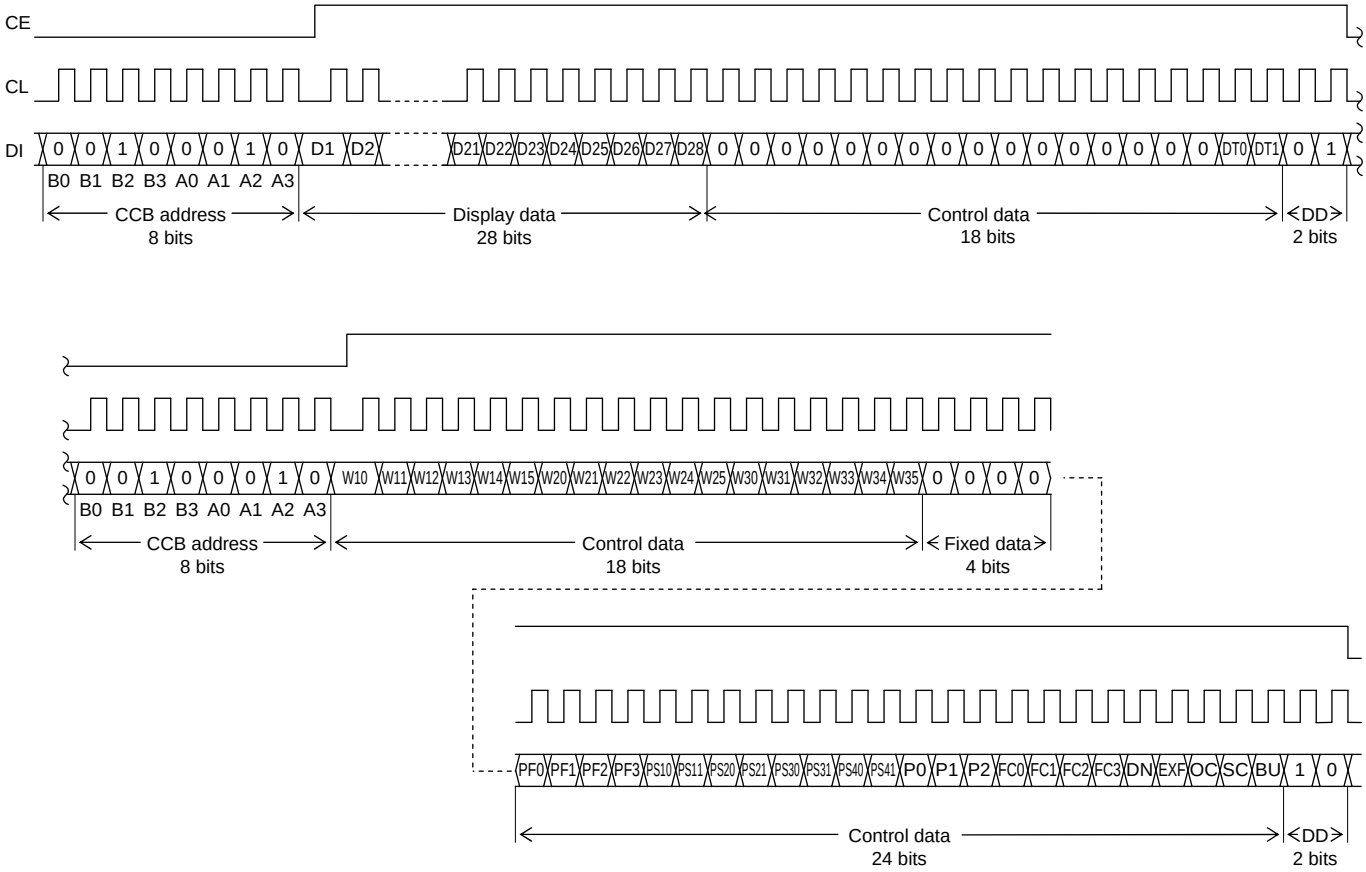
- EXF ..... External clock operating frequency setting control data
- OC ..... Internal oscillator operating mode/external clock operating mode switching control data
- SC ..... Segment on/off control data
- BU ..... Normal mode/power-saving mode control data

4. 1/1 duty

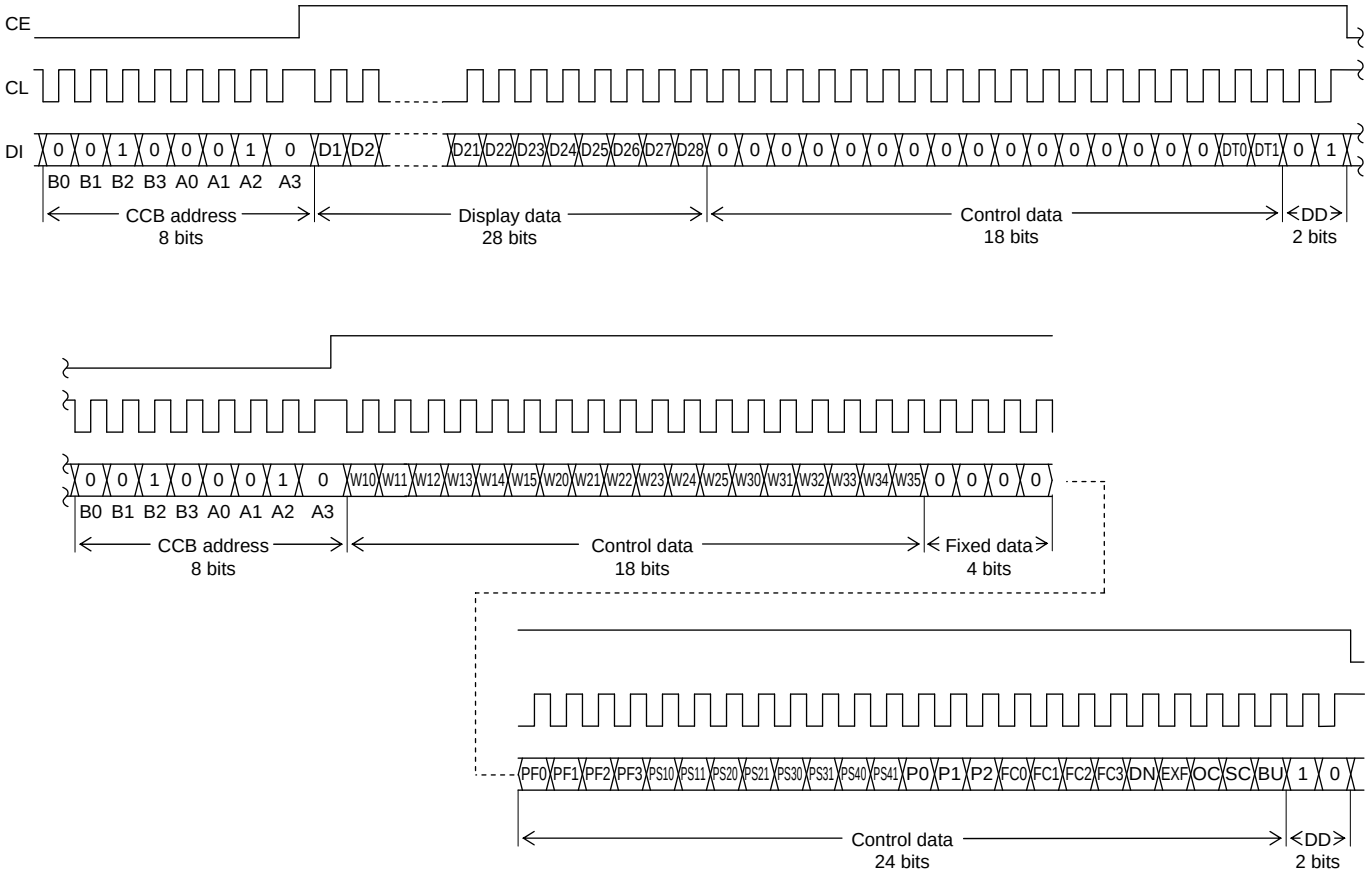
(1) When CL is stopped at the low level



Note: DD is the direction data

- CCB address ..... "44H"
- D1 to D28 ..... Display data
- DT0, DT1 ..... 1/1-duty to 1/4-duty drive switching control data
- W 10 to W15, W20 to W25, W30 to W35 ... PWM data of the PWM output
- PF0 to PF3 ..... PWM output waveform frame frequency setting control data
- PS10, PS11 to PS40, PS41 ..... General-purpose output port (P1 to P4) function setting control data
- P0 to P2 ..... Segment output port/general-purpose output port switching control data
- FC0 to FC3 ..... Common/segment output waveform frame frequency setting control data
- DN ..... S28 pin state setting control data
- EXF ..... External clock operating frequency setting control data
- OC ..... Internal oscillator operating mode/external clock operating mode switching control data
- SC ..... Segment on/off control data
- BU ..... Normal mode/power-saving mode control data

(2) When CL is stopped at the high level



Note: DD is the direction data

- CCB address ..... "44H"
- D1 to D28 ..... Display data
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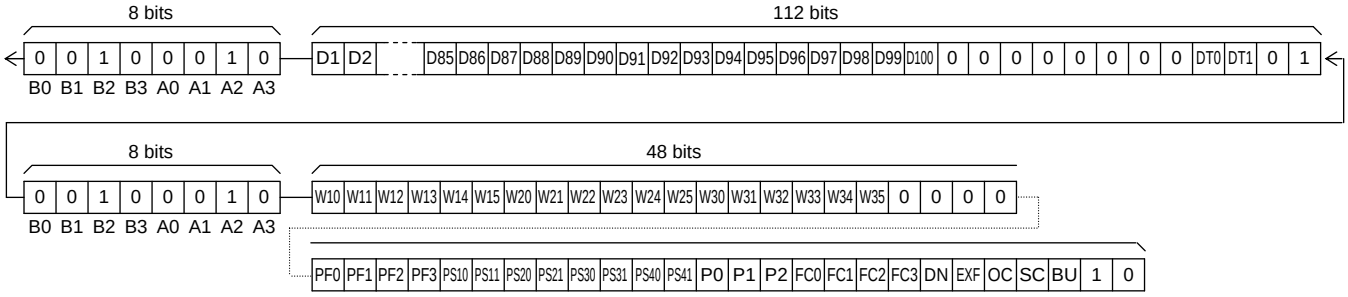
- W 10 to W15, W20 to W25, W30 to W35 ... PWM data of the PWM output
- PF0 to PF3 ..... PWM output waveform frame frequency setting control data
- PS10, PS11 to PS40, PS41 ..... General-purpose output port (P1 to P4) function setting control data
- P0 to P2 ..... Segment output port/general-purpose output port switching control data
- FC0 to FC3 ..... Common/segment output waveform frame frequency setting control data
- DN ..... S28 pin state setting control data
- EXF ..... External clock operating frequency setting control data
- OC ..... Internal oscillator operating mode/external clock operating mode switching control data
- SC ..... Segment on/off control data
- BU ..... Normal mode/power-saving mode control data

Serial Data Transfer Example

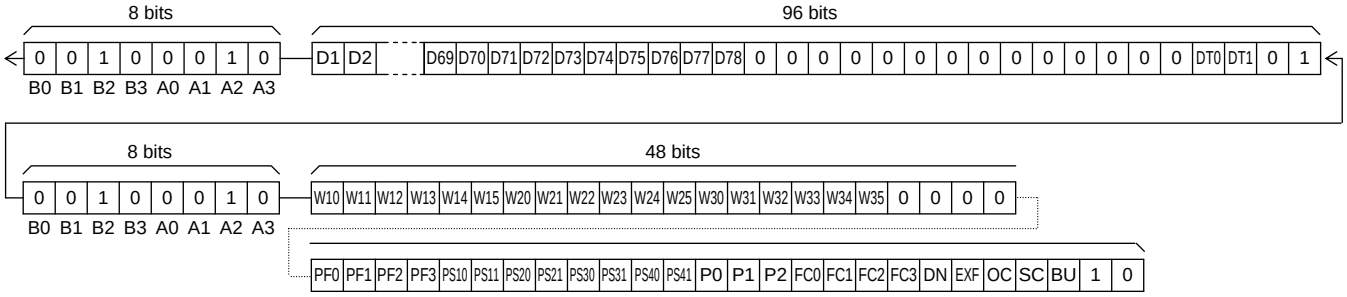
1. 1/4 duty

All 160 bits of serial data must be sent.



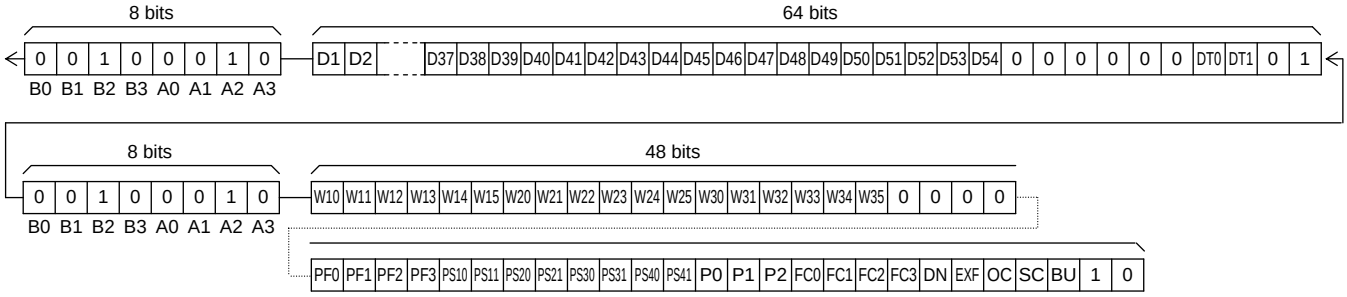
2. 1/3 duty

All 144 bits of serial data must be sent.



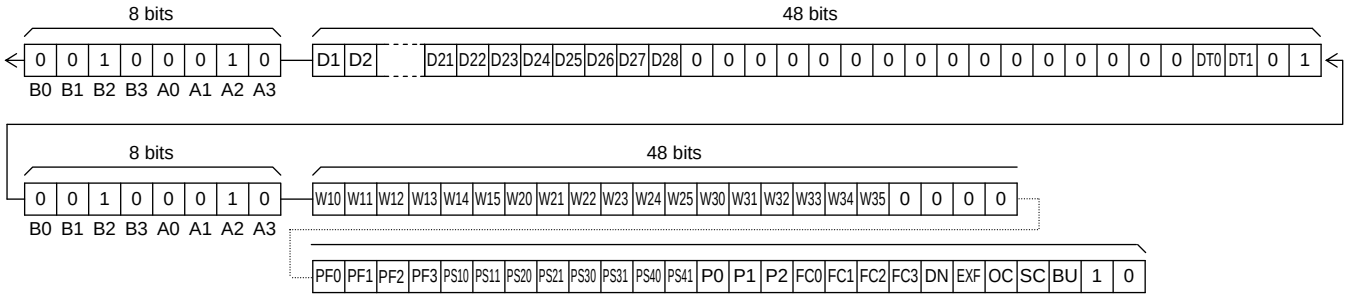
3. 1/2 duty

All 112 bits of serial data must be sent.



4. 1/1 duty

All 96 bits of serial data must be sent.



Control Data Functions

(1) DT0, DT1 · · · LCD drive scheme (1/1-duty to 1/4-duty drive) switching control data.

These control data bits select 1/4-duty 1/3 bias drive, 1/3-duty 1/3 bias drive, 1/2-duty 1/2 bias drive, or 1/1-duty drive.

DT0	DT1	Drive scheme	Pin state		
			COM2/S27	COM3/S26	COM4/S25
0	0	1/4-duty 1/3-bias drive	COM2	COM3	COM4
1	0	1/3-duty 1/3-bias drive	COM2	COM3	S25
0	1	1/2-duty 1/2-bias drive	COM2	S26	S25
1	1	static (1/1-duty drive)	S27	S26	S25

Note: COM2 to COM4: Common output , S27 to S25: Segment output

(2) PF0 to PF3 · · · PWM output waveform frame frequency setting control data

These control data bits set the frame frequency of the PWM output waveforms. However, when the PWM output function isn't used, these control data bits become invalid. In addition, when the external clock operating frequency is set the $f_{CK}2$=38[KHz] typ (EXF="1") in external clock operating mode (OC="1"), these control data bits become invalid.

Control data				PWM output waveform frame frequency fp[Hz]	
PF0	PF1	PF2	PF3	Internal oscillator operating mode (The control data OC is 0, fosc=300[kHz]typ)	External clock operating mode (The control data OC is 1, and EXF is 0, $f_{CK}1$=300[kHz]typ)
0	0	0	0	fosc/1536	$f_{CK}1$/1536
1	0	0	0	fosc/1408	$f_{CK}1$/1408
0	1	0	0	fosc/1280	$f_{CK}1$/1280
1	1	0	0	fosc/1152	$f_{CK}1$/1152
0	0	1	0	fosc/1024	$f_{CK}1$/1024
1	0	1	0	fosc/896	$f_{CK}1$/896
0	1	1	0	fosc/768	$f_{CK}1$/768
1	1	1	0	fosc/640	$f_{CK}1$/640
0	0	0	1	fosc/512	$f_{CK}1$/512
1	0	0	1	fosc/384	$f_{CK}1$/384
0	1	0	1	fosc/256	$f_{CK}1$/256

Note: When is setting (PF0, PF1, PF2, PF3)=(1, 1, 0, 1) and (X, X, 1, 1), the frame frequency is same as frame frequency at the time of the (PF0, PF1, PF2, PF3)=(1, 0, 1, 0) setting (fosc/896, $f_{CK}1$/896).

X : don't care

(3) PS10, PS11 to PS40, PS41 · · · General-purpose output port (P1 to P4) function setting control data

These control data bits set the general-purpose output function (High or low level output), clock output function or PWM output function of the P1 output pin, and the general-purpose output function (High or low level output) or PWM output function of the P2 to P4 output pins.

However, be careful of being unable to set a PWM output function when the external clock operating frequency is set the f_{CK}2=38[kHz] typ (EXF="1") in external clock operating mode (OC="1").

PS10	PS11	General-purpose output port (P1) function
0	0	General-purpose output function (High or low level output)
1	0	Clock output function (clock frequency : fosc/2, f_{CK}/2)
0	1	Clock output function (clock frequency : fosc/8, f_{CK}/8)
1	1	PWM output function (ch1) (Support for PWM data W10 to W15)

PS20	PS21	General-purpose output port (P2) function
0	0	General-purpose output function (High or low level output)
1	0	PWM output function (ch1) (Support for PWM data W10 to W15)
0	1	PWM output function (ch2) (Support for PWM data W20 to W25)
1	1	PWM output function (ch3) (Support for PWM data W30 to W35)

PS30	PS31	General-purpose output port (P3) function
0	0	General-purpose output function (High or low level output)
1	0	PWM output function (ch1) (Support for PWM data W10 to W15)
0	1	PWM output function (ch2) (Support for PWM data W20 to W25)
1	1	PWM output function (ch3) (Support for PWM data W30 to W35)

PS40	PS41	General-purpose output port (P4) function
0	0	General-purpose output function (High or low level output)
1	0	PWM output function (ch1) (Support for PWM data W10 to W15)
0	1	PWM output function (ch2) (Support for PWM data W20 to W25)
1	1	PWM output function (ch3) (Support for PWM data W30 to W35)

(4) P0 to P2 · · · Segment output port/general-purpose output port switching control data.

These control data bits switch the segment output port/general-purpose output port functions of the S1/P1 to S4/P4 output pins.

Control data			Output pin state			
P0	P1	P2	S1/P1	S2/P2	S3/P3	S4/P4
0	0	0	S1	S2	S3	S4
0	0	1	P1	S2	S3	S4
0	1	0	P1	P2	S3	S4
0	1	1	P1	P2	P3	S4
1	0	0	P1	P2	P3	P4

Note: Sn(n=1 to 4): Segment output ports
Pn(n=1 to 4): General-purpose output ports

Note: When are setting (P0, P1, P2)=(1, 0, 1), (1, 1, 0), and (1, 1, 1), the all P1/S1 to P4/S4 output pins selects the segment output port.

The table below lists the correspondence between the display data and the output pins when these pins are selected to be general-purpose output ports.

Output pin	Correspondence display data			
	1/4 duty	1/3 duty	1/2 duty	1/1 duty
S1/P1	D1	D1	D1	D1
S2/P2	D5	D4	D3	D2
S3/P3	D9	D7	D5	D3
S4/P4	D13	D10	D7	D4

For example, if the circuit is operated in 1/4 duty and the S4/P4 output pin is selected to be a general-purpose output port, the S4/P4 output pin will output a high level when the display data D13 is 1, and will output a low level when D13 is 0.

(5) FC0 to FC3 · · · Common/segment output waveform frame frequency control data

These control data bits set the frame frequency of the common and segment output waveforms.

Control data				Frame frequency fo[Hz]		
FC0	FC1	FC2	FC3	Internal oscillator operating mode (The control data OC is 0, fosc=300[kHz]typ)	External clock operating mode (The control data OC is 1, and EXF is 0, $f_{CK}1$=300[kHz]typ)	External clock operating mode (The control data OC is 1, and EXF is 1, $f_{CK}2$=38[kHz]typ)
0	0	0	0	fosc/6144	$f_{CK}1/6144$	$f_{CK}2/768$
0	0	0	1	fosc/5376	$f_{CK}1/5376$	$f_{CK}2/672$
0	0	1	0	fosc/4608	$f_{CK}1/4608$	$f_{CK}2/576$
0	0	1	1	fosc/3840	$f_{CK}1/3840$	$f_{CK}2/480$
0	1	0	0	fosc/3456	$f_{CK}1/3456$	$f_{CK}2/432$
0	1	0	1	fosc/3072	$f_{CK}1/3072$	$f_{CK}2/384$
0	1	1	0	fosc/2688	$f_{CK}1/2688$	$f_{CK}2/336$
0	1	1	1	fosc/2304	$f_{CK}1/2304$	$f_{CK}2/288$
1	0	0	0	fosc/2112	$f_{CK}1/2112$	$f_{CK}2/264$
1	0	0	1	fosc/1920	$f_{CK}1/1920$	$f_{CK}2/240$
1	0	1	0	fosc/1728	$f_{CK}1/1728$	$f_{CK}2/216$
1	0	1	1	fosc/1536	$f_{CK}1/1536$	$f_{CK}2/192$
1	1	0	0	fosc/1344	$f_{CK}1/1344$	$f_{CK}2/168$
1	1	0	1	fosc/1152	$f_{CK}1/1152$	$f_{CK}2/144$
1	1	1	0	fosc/960	$f_{CK}1/960$	$f_{CK}2/120$
1	1	1	1	fosc/768	$f_{CK}1/768$	$f_{CK}2/96$

(6) DN · · · S28 pin state setting control data

This control data bit sets state of the S28 pin.

DN	Number of display segments				Pin state
	1/4 duty	1/3 duty	1/2 duty	1/1 duty	S28
0	Up to 96 segments	Up to 75 segments	Up to 52 segments	Up to 27 segments	"L" (V_{SS})
1	Up to100 segments	Up to 78 segments	Up to 54 segments	Up to 28 segments	S28

(7) EXF · · · External clock operating frequency setting control data

This control data sets the operating frequency of the external clock which input into the OSCI pin, when the external clock operating mode (OC="1") is set. However, this control data is effective only when external clock operating mode (OC="1") is set.

EXF	External clock operating frequency f_{CK}[KHz]
0	$f_{CK}1$=300[kHz]typ
1	$f_{CK}2$=38[kHz]typ

(8) OC · · · Internal oscillator operating mode/external clock operating mode switching control data.

This control data bit selects either the internal oscillator operating mode or external clock operating mode.

OC	Fundamental clock operating mode	Input pin (OSCI) state
0	Internal oscillator operating mode	Connect to GND
1	External clock operating mode	Input the clock from the outside

(9) SC · · · Segment on/off control data

This control data bit controls the on/off state of the segments.

SC	Display state
0	on
1	off

Note that when the segments are turned off by setting SC to 1, the segments are turned off by outputting segment off waveforms from the segment output pins.

(10) BU · · · Normal mode/power-saving mode control data

This control data bit selects either normal mode or power-saving mode.

BU	Mode
0	Normal mode
1	Power saving mode In this mode, the internal oscillator circuit stops oscillation if the IC is in the internal oscillator operating mode(OC=0) and the IC stops receiving external clock signals if the IC is in the external clock operating mode(OC=1). The common and segment output pins go to the V_{SS} level. However, the S1/P1 to S4/P4 output pins can be used as general-purpose output ports under the control of the data bits P0 to P2. (The general-purpose output port P1 to P4 can not be used as clock output or PWM output).

(11) W10 to W15, W20 to W25, W30 to W35 · · · PWM data of the PWM output

These control data bits set the pulse width of the PWM output P1 to P4. However, when the PWM output function isn't used, these control data bits become invalid. In addition, when the external clock operating frequency is set the f_{CK}2=38[kHz]typ (EXF="1") in external clock operating mode (OC="1"), these control data bits become invalid.

Wn0	Wn1	Wn2	Wn3	Wn4	Wn5	Pulse width of PWM output
0	0	0	0	0	0	(1/64)×Tp
1	0	0	0	0	0	(2/64)×Tp
0	1	0	0	0	0	(3/64)×Tp
1	1	0	0	0	0	(4/64)×Tp
0	0	1	0	0	0	(5/64)×Tp
1	0	1	0	0	0	(6/64)×Tp
0	1	1	0	0	0	(7/64)×Tp
1	1	1	0	0	0	(8/64)×Tp
0	0	0	1	0	0	(9/64)×Tp
1	0	0	1	0	0	(10/64)×Tp
0	1	0	1	0	0	(11/64)×Tp
1	1	0	1	0	0	(12/64)×Tp
0	0	1	1	0	0	(13/64)×Tp
1	0	1	1	0	0	(14/64)×Tp
0	1	1	1	0	0	(15/64)×Tp
1	1	1	1	0	0	(16/64)×Tp
0	0	0	0	1	0	(17/64)×Tp
1	0	0	0	1	0	(18/64)×Tp
0	1	0	0	1	0	(19/64)×Tp
1	1	0	0	1	0	(20/64)×Tp
0	0	1	0	1	0	(21/64)×Tp
1	0	1	0	1	0	(22/64)×Tp
0	1	1	0	1	0	(23/64)×Tp
1	1	1	0	1	0	(24/64)×Tp
0	0	0	1	1	0	(25/64)×Tp
1	0	0	1	1	0	(26/64)×Tp
0	1	0	1	1	0	(27/64)×Tp
1	1	0	1	1	0	(28/64)×Tp
0	0	1	1	1	0	(29/64)×Tp
1	0	1	1	1	0	(30/64)×Tp
0	1	1	1	1	0	(31/64)×Tp
1	1	1	1	1	0	(32/64)×Tp

Wn0	Wn1	Wn2	Wn3	Wn4	Wn5	Pulse width of PWM output
0	0	0	0	0	1	(33/64)×Tp
1	0	0	0	0	1	(34/64)×Tp
0	1	0	0	0	1	(35/64)×Tp
1	1	0	0	0	1	(36/64)×Tp
0	0	1	0	0	1	(37/64)×Tp
1	0	1	0	0	1	(38/64)×Tp
0	1	1	0	0	1	(39/64)×Tp
1	1	1	0	0	1	(40/64)×Tp
0	0	0	1	0	1	(41/64)×Tp
1	0	0	1	0	1	(42/64)×Tp
0	1	0	1	0	1	(43/64)×Tp
1	1	0	1	0	1	(44/64)×Tp
0	0	1	1	0	1	(45/64)×Tp
1	0	1	1	0	1	(46/64)×Tp
0	1	1	1	0	1	(47/64)×Tp
1	1	1	1	0	1	(48/64)×Tp
0	0	0	0	1	1	(49/64)×Tp
1	0	0	0	1	1	(50/64)×Tp
0	1	0	0	1	1	(51/64)×Tp
1	1	0	0	1	1	(52/64)×Tp
0	0	1	0	1	1	(53/64)×Tp
1	0	1	0	1	1	(54/64)×Tp
0	1	1	0	1	1	(55/64)×Tp
1	1	1	0	1	1	(56/64)×Tp
0	0	0	1	1	1	(57/64)×Tp
1	0	0	1	1	1	(58/64)×Tp
0	1	0	1	1	1	(59/64)×Tp
1	1	0	1	1	1	(60/64)×Tp
0	0	1	1	1	1	(61/64)×Tp
1	0	1	1	1	1	(62/64)×Tp
0	1	1	1	1	1	(63/64)×Tp
1	1	1	1	1	1	(64/64)×Tp

Note : W10 to W15 · · · PWM data of the PWM output (Ch1)
W20 to W25 · · · PWM data of the PWM output (Ch2)
W30 to W35 · · · PWM data of the PWM output (Ch3)

n=1 to 3

$$Tp = \frac{1}{fp}$$

Display Data and Output Pin Correspondence (1/4 Duty)

Output pin	COM1	COM2	COM3	COM4
S1/P1	D1	D2	D3	D4
S2/P2	D5	D6	D7	D8
S3/P3	D9	D10	D11	D12
S4/P4	D13	D14	D15	D16
S5	D17	D18	D19	D20
S6	D21	D22	D23	D24
S7	D25	D26	D27	D28
S8	D29	D30	D31	D32
S9	D33	D34	D35	D36
S10	D37	D38	D39	D40
S11	D41	D42	D43	D44
S12	D45	D46	D47	D48
S13	D49	D50	D51	D52

Output pin	COM1	COM2	COM3	COM4
S14	D53	D54	D55	D56
S15	D57	D58	D59	D60
S16	D61	D62	D63	D64
S17	D65	D66	D67	D68
S18	D69	D70	D71	D72
S19	D73	D74	D75	D76
S20	D77	D78	D79	D80
S21	D81	D82	D83	D84
S22	D85	D86	D87	D88
S23	D89	D90	D91	D92
S24	D93	D94	D95	D96
S28	D97	D98	D99	D100

Note: This table assumes that pins S1/P1 to S4/P4 are configured for segment output.

For example, the table below lists the output states for the S21 output pin.

Display data				Output pin (S21) state
D81	D82	D83	D84	
0	0	0	0	The LCD segments corresponding to COM1, COM2, COM3, and COM4 are off.
0	0	0	1	The LCD segment corresponding to COM4 is on.
0	0	1	0	The LCD segment corresponding to COM3 is on.
0	0	1	1	The LCD segments corresponding to COM3 and COM4 are on.
0	1	0	0	The LCD segment corresponding to COM2 is on.
0	1	0	1	The LCD segments corresponding to COM2 and COM4 are on.
0	1	1	0	The LCD segments corresponding to COM2 and COM3 are on.
0	1	1	1	The LCD segments corresponding to COM2, COM3, and COM4 are on.
1	0	0	0	The LCD segment corresponding to COM1 is on.
1	0	0	1	The LCD segments corresponding to COM1 and COM4 are on.
1	0	1	0	The LCD segments corresponding to COM1 and COM3 are on.
1	0	1	1	The LCD segments corresponding to COM1, COM3, and COM4 are on.
1	1	0	0	The LCD segments corresponding to COM1 and COM2 are on.
1	1	0	1	The LCD segments corresponding to COM1, COM2, and COM4 are on.
1	1	1	0	The LCD segments corresponding to COM1, COM2, and COM3 are on.
1	1	1	1	The LCD segments corresponding to COM1, COM2, COM3, and COM4 are on.

Display Data and Output Pin Correspondence (1/3 Duty)

Output pin	COM1	COM2	COM3
S1/P1	D1	D2	D3
S2/P2	D4	D5	D6
S3/P3	D7	D8	D9
S4/P4	D10	D11	D12
S5	D13	D14	D15
S6	D16	D17	D18
S7	D19	D20	D21
S8	D22	D23	D24
S9	D25	D26	D27
S10	D28	D29	D30
S11	D31	D32	D33
S12	D34	D35	D36
S13	D37	D38	D39

Output pin	COM1	COM2	COM3
S14	D40	D41	D42
S15	D43	D44	D45
S16	D46	D47	D48
S17	D49	D50	D51
S18	D52	D53	D54
S19	D55	D56	D57
S20	D58	D59	D60
S21	D61	D62	D63
S22	D64	D65	D66
S23	D67	D68	D69
S24	D70	D71	D72
COM4/S25	D73	D74	D75
S28	D76	D77	D78

Note: This table assumes that pins S1/P1 to S4/P4, and COM4/S25 are configured for segment output.

For example, the table below lists the output states for the S21 output pin.

Display data			Output pin (S21) state
D61	D62	D63	
0	0	0	The LCD segments corresponding to COM1, COM2 and COM3 are off.
0	0	1	The LCD segment corresponding to COM3 is on.
0	1	0	The LCD segment corresponding to COM2 is on.
0	1	1	The LCD segments corresponding to COM2 and COM3 are on.
1	0	0	The LCD segment corresponding to COM1 is on.
1	0	1	The LCD segments corresponding to COM1 and COM3 are on.
1	1	0	The LCD segments corresponding to COM1 and COM2 are on.
1	1	1	The LCD segments corresponding to COM1, COM2, and COM3 are on.

Display Data and Output Pin Correspondence (1/2 Duty)

Output pin	COM1	COM2
S1/P1	D1	D2
S2/P2	D3	D4
S3/P3	D5	D6
S4/P4	D7	D8
S5	D9	D10
S6	D11	D12
S7	D13	D14
S8	D15	D16
S9	D17	D18
S10	D19	D20
S11	D21	D22
S12	D23	D24
S13	D25	D26
S14	D27	D28

Output pin	COM1	COM2
S15	D29	D30
S16	D31	D32
S17	D33	D34
S18	D35	D36
S19	D37	D38
S20	D39	D40
S21	D41	D42
S22	D43	D44
S23	D45	D46
S24	D47	D48
COM4/S25	D49	D50
COM3/S26	D51	D52
S28	D53	D54

Note: This table assumes that pins S1/P1 to S4/P4, COM4/S25, and COM3/S26 are configured for segment output.

For example, the table below lists the output states for the S21 output pin.

Display data		Output pin (S21) state
D41	D42	
0	0	The LCD segments corresponding to COM1 and COM2 are off.
0	1	The LCD segment corresponding to COM2 is on.
1	0	The LCD segment corresponding to COM1 is on.
1	1	The LCD segments corresponding to COM1 and COM2 are on.

Display Data and Output Pin Correspondence (1/1 Duty)

Output pin	COM1
S1/P1	D1
S2/P2	D2
S3/P3	D3
S4/P4	D4
S5	D5
S6	D6
S7	D7
S8	D8
S9	D9
S10	D10
S11	D11
S12	D12
S13	D13
S14	D14

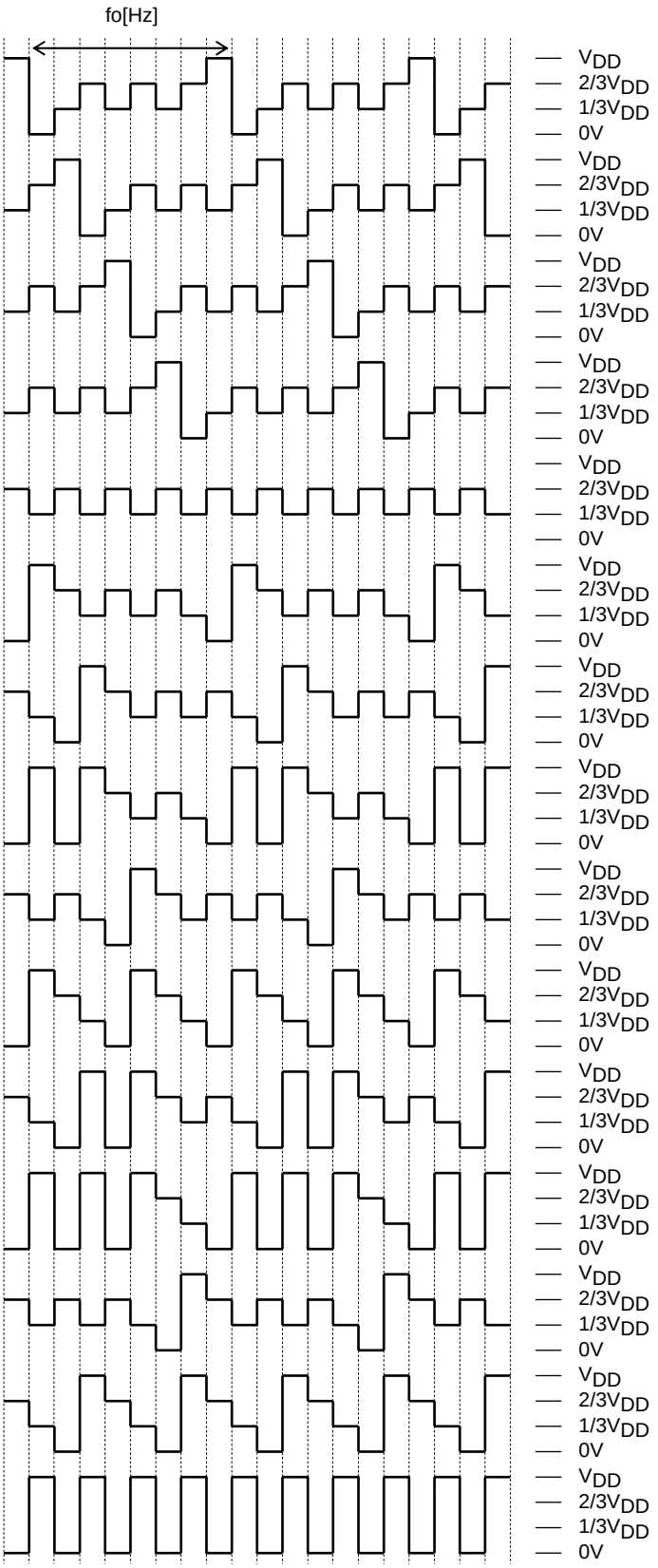
Output pin	COM1
S15	D15
S16	D16
S17	D17
S18	D18
S19	D19
S20	D20
S21	D21
S22	D22
S23	D23
S24	D24
COM4/S25	D25
COM3/S26	D26
COM2/S27	D27
S28	D28

Note: This table assumes that pins S1/P1 to S4/P4, COM4/S25, COM3/S26, and COM2/S27 are configured for segment output.

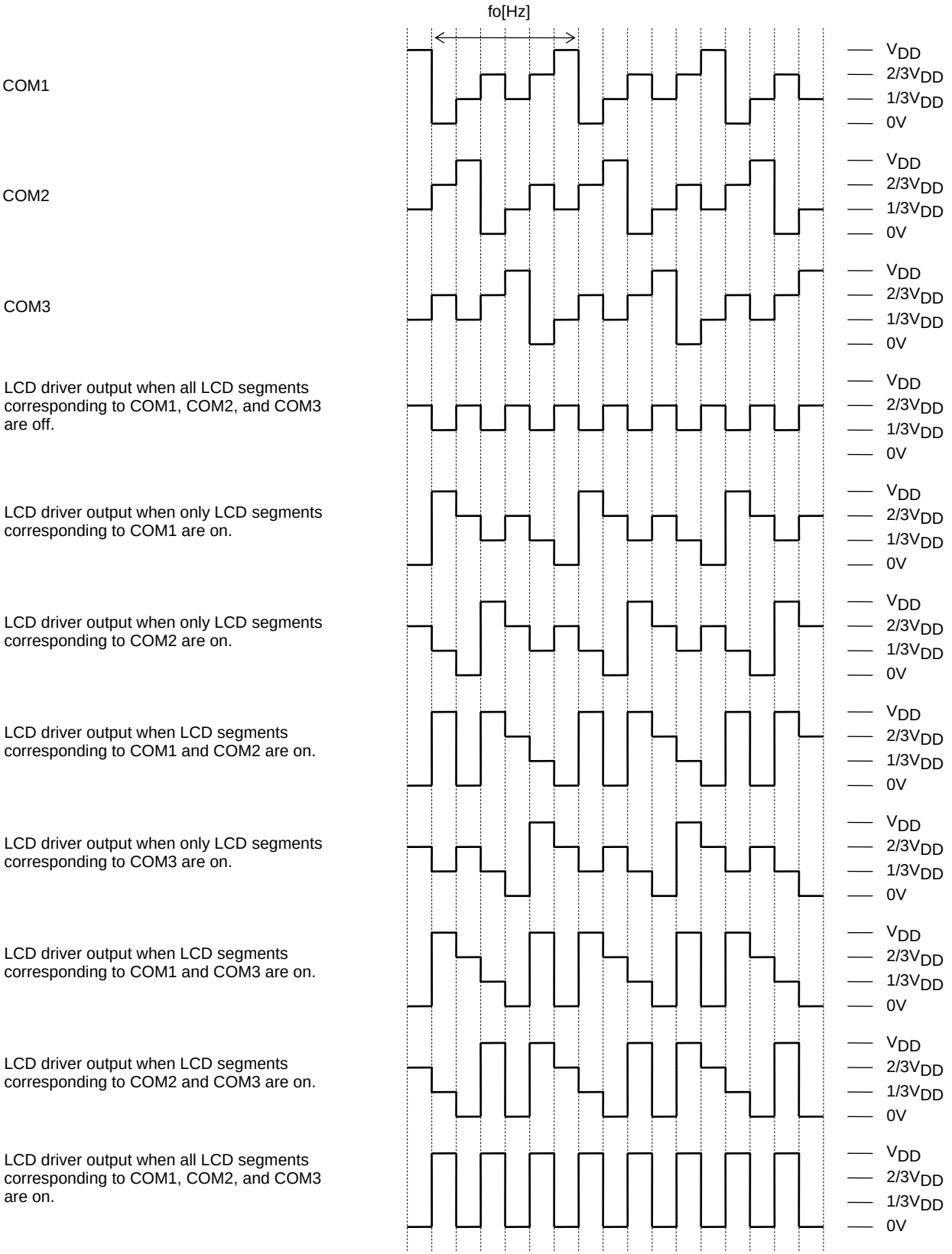
For example, the table below lists the output states for the S21 output pin.

Display data	Output pin (S21) state
D21	
0	The LCD segment corresponding to COM1 is off.
1	The LCD segment corresponding to COM1 is on.

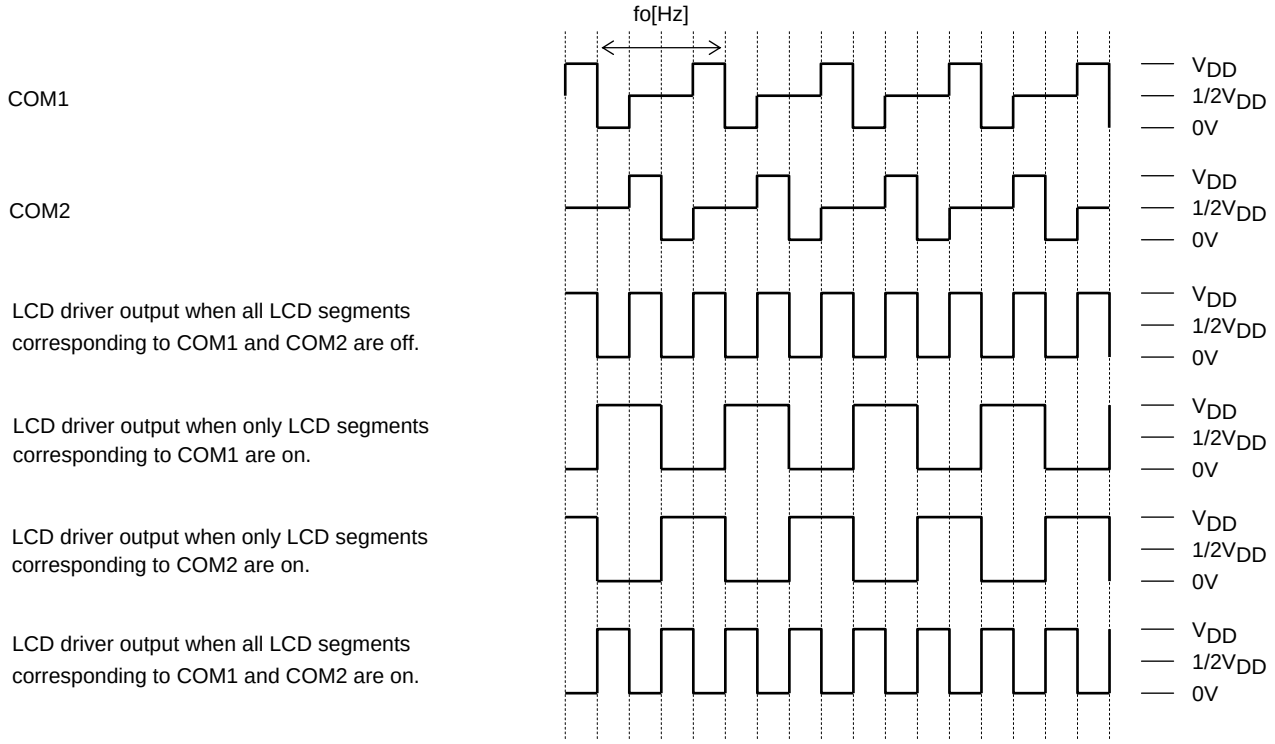
Output waveforms (1/4-Duty 1/3-Bias Drive Scheme)



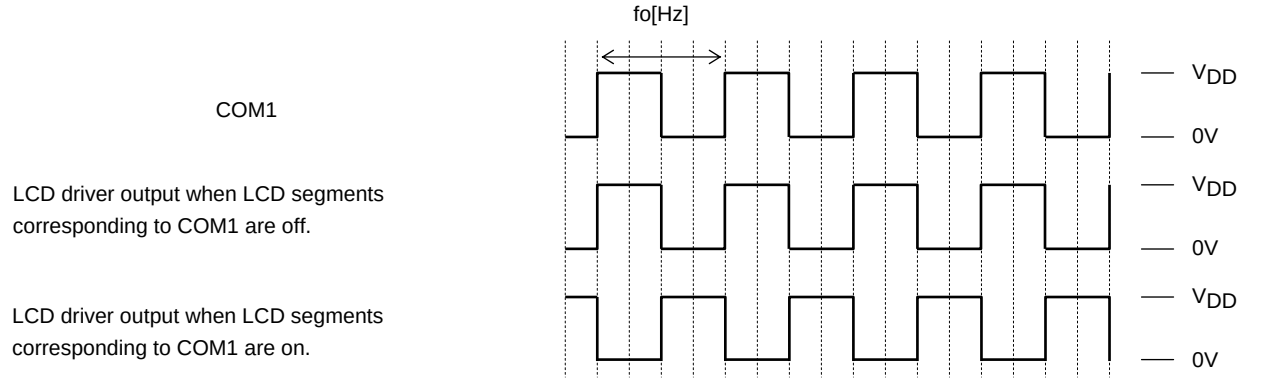
Output waveforms (1/3-Duty 1/3-Bias Drive Scheme)



Output waveforms (1/2-Duty 1/2-Bias Drive Scheme)

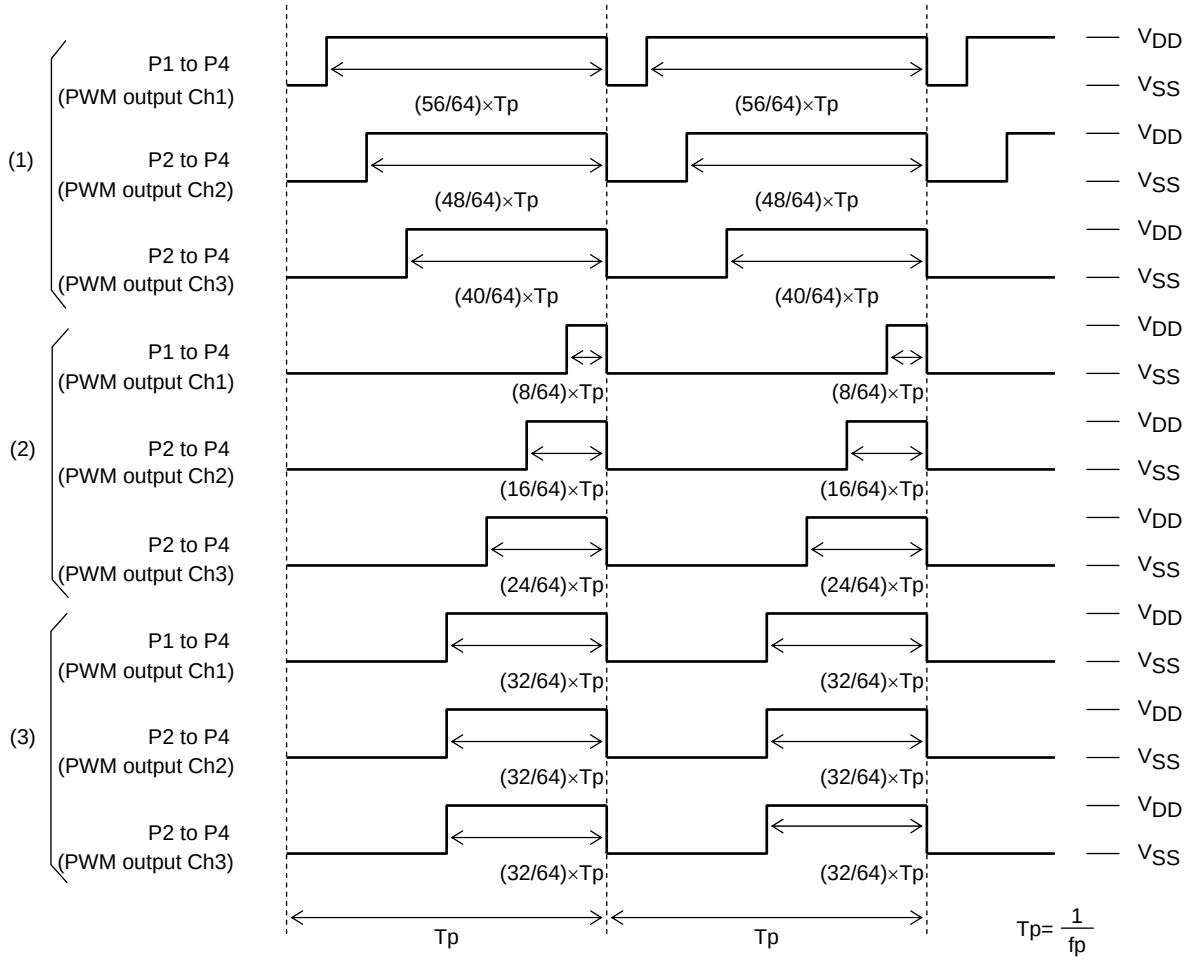


Output waveforms (1/1-Duty Drive Scheme)



Control data				Frame frequency fo[Hz]		
FC0	FC1	FC2	FC3	Internal oscillator operating mode (The control data OC is 0, fosc=300[kHz]typ)	External clock operating mode (The control data OC is 1, and EXF is 0, $f_{CK}1$=300[kHz]typ)	External clock operating mode (The control data OC is 1, and EXF is 1, $f_{CK}2$=38[kHz]typ)
0	0	0	0	fosc/6144	$f_{CK}1$/6144	$f_{CK}2$/768
0	0	0	1	fosc/5376	$f_{CK}1$/5376	$f_{CK}2$/672
0	0	1	0	fosc/4608	$f_{CK}1$/4608	$f_{CK}2$/576
0	0	1	1	fosc/3840	$f_{CK}1$/3840	$f_{CK}2$/480
0	1	0	0	fosc/3456	$f_{CK}1$/3456	$f_{CK}2$/432
0	1	0	1	fosc/3072	$f_{CK}1$/3072	$f_{CK}2$/384
0	1	1	0	fosc/2688	$f_{CK}1$/2688	$f_{CK}2$/336
0	1	1	1	fosc/2304	$f_{CK}1$/2304	$f_{CK}2$/288
1	0	0	0	fosc/2112	$f_{CK}1$/2112	$f_{CK}2$/264
1	0	0	1	fosc/1920	$f_{CK}1$/1920	$f_{CK}2$/240
1	0	1	0	fosc/1728	$f_{CK}1$/1728	$f_{CK}2$/216
1	0	1	1	fosc/1536	$f_{CK}1$/1536	$f_{CK}2$/192
1	1	0	0	fosc/1344	$f_{CK}1$/1344	$f_{CK}2$/168
1	1	0	1	fosc/1152	$f_{CK}1$/1152	$f_{CK}2$/144
1	1	1	0	fosc/960	$f_{CK}1$/960	$f_{CK}2$/120
1	1	1	1	fosc/768	$f_{CK}1$/768	$f_{CK}2$/96

PWM output waveforms



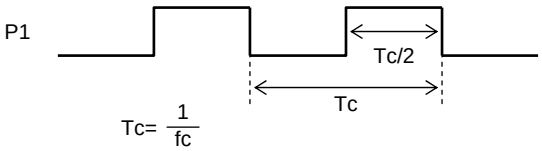
Control data																		PWM output waveforms
W10	W11	W12	W13	W14	W15	W20	W21	W22	W23	W24	W25	W30	W31	W32	W33	W34	W35	
1	1	1	0	1	1	1	1	1	1	0	1	1	1	1	0	0	1	(1)
1	1	1	0	0	0	1	1	1	1	0	0	1	1	1	0	1	0	(2)
1	1	1	1	1	0	1	1	1	1	1	0	1	1	1	1	1	0	(3)

Control data				PWM output waveform frame frequency fp[Hz]	
PF0	PF1	PF2	PF3	Internal oscillator operating mode (The control data OC is 0, fosc=300[kHz]typ)	External clock operating mode (The control data OC is 1, and EXF is 0, f_{CK}1=300[kHz]typ)
0	0	0	0	fosc/1536	f_{CK}1/1536
1	0	0	0	fosc/1408	f_{CK}1/1408
0	1	0	0	fosc/1280	f_{CK}1/1280
1	1	0	0	fosc/1152	f_{CK}1/1152
0	0	1	0	fosc/1024	f_{CK}1/1024
1	0	1	0	fosc/896	f_{CK}1/896
0	1	1	0	fosc/768	f_{CK}1/768
1	1	1	0	fosc/640	f_{CK}1/640
0	0	0	1	fosc/512	f_{CK}1/512
1	0	0	1	fosc/384	f_{CK}1/384
0	1	0	1	fosc/256	f_{CK}1/256

Note: When is setting (PF0, PF1, PF2, PF3)=(1, 1, 0, 1) and (X, X, 1, 1) the frame frequency is same as frame frequency at the time of the (PF0, PF1, PF2, PF3)=(1, 0, 1, 0) setting (fosc/896, f_{CK}1/896).

X:don't care

Clock output waveforms



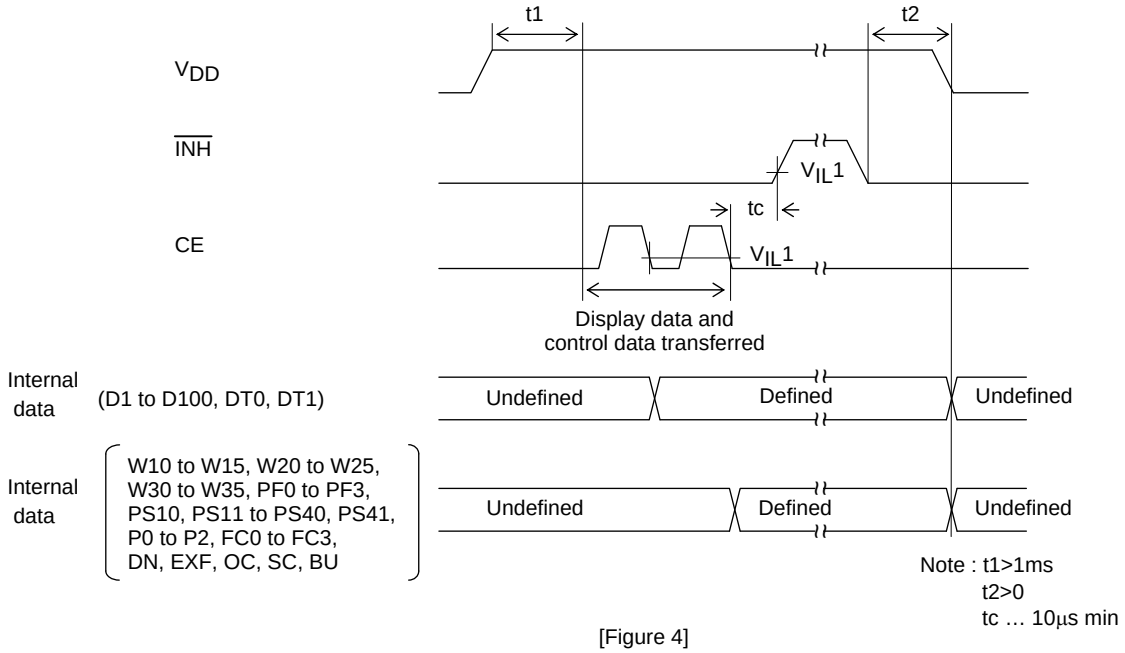
$Tc = \frac{1}{fc}$

Control data		Clock frequency of clock output P1 fc(=1/Tc)[Hz]
PS10	PS11	
1	0	Clock output function (fosc/2, f_{CK}/2)
0	1	Clock output function (fosc/8, f_{CK}/8)

Display Control and the $\overline{INH}$ Pin

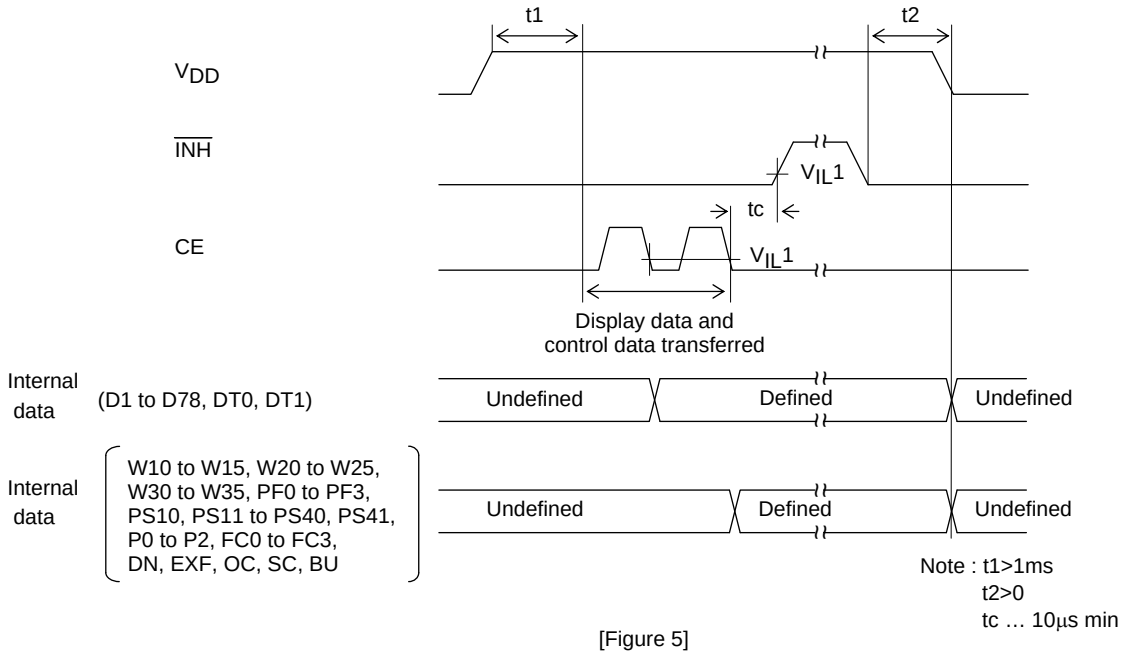
Since the LSI internal data (1/4 duty : the display data D1 to D100 and the control data, 1/3 duty : the display data D1 to D78 and the control data, 1/2 duty : the display data D1 to D54 and the control data, 1/1 duty : the display data D1 to D28 and the control data) is undefined when power is first applied, applications should set the $\overline{INH}$ pin low at the same time as power is applied to turn off the display (This sets the S1/P1 to S4/P4, S5 to S24, COM4/S25, COM3/S26,COM2/S27, COM1, and S28 pins to the V_{SS} level.) and during this period send serial data from the controller. The controller should then set the $\overline{INH}$ pin high after the data transfer has completed . This procedure prevents meaningless display at power on. (See Figure 4, Figure 5, Figure 6, Figure 7.)

(1)1/4 duty



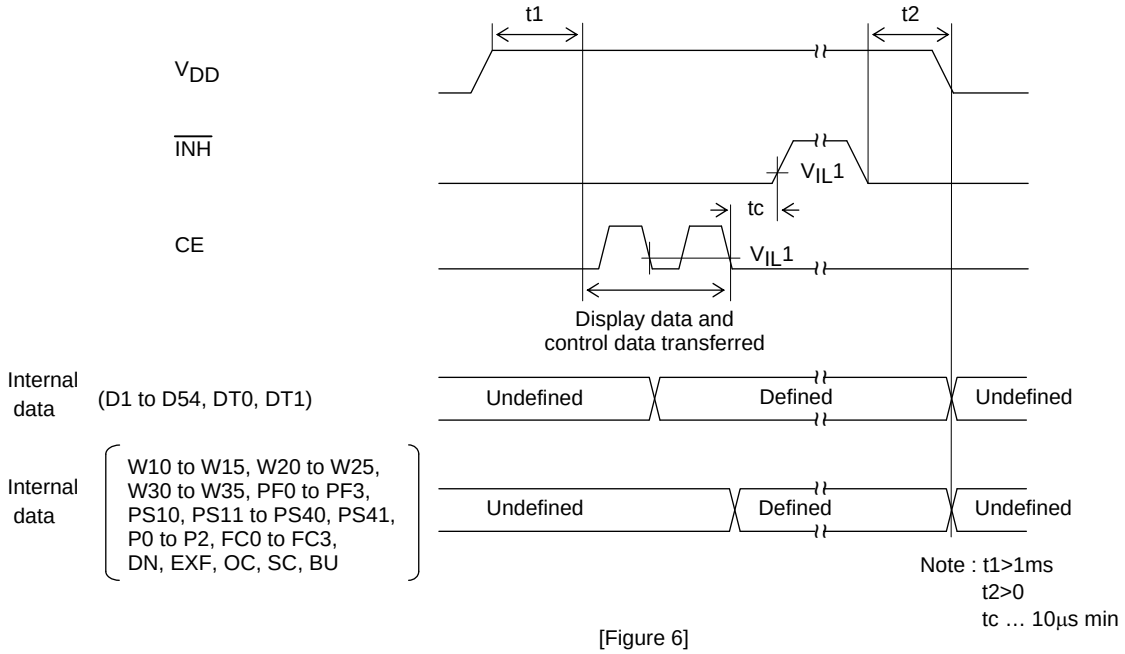
[Figure 4]

(2)1/3 duty



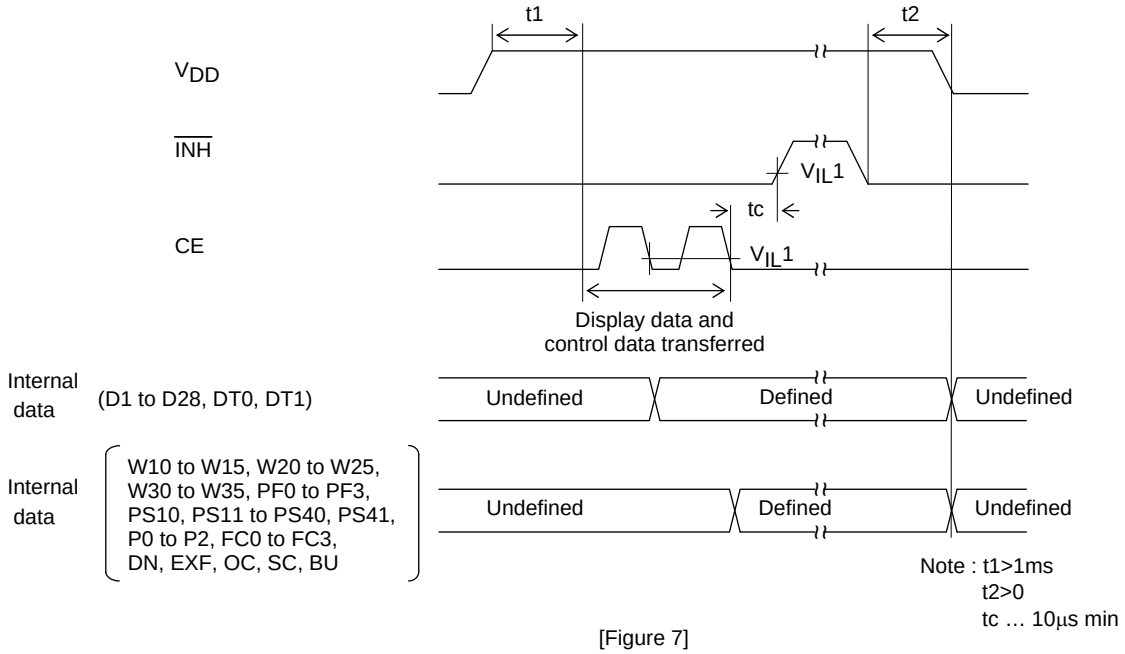
[Figure 5]

(3)1/2 duty



[Figure 6]

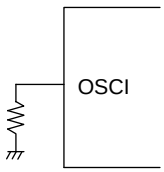
(4)1/1 duty



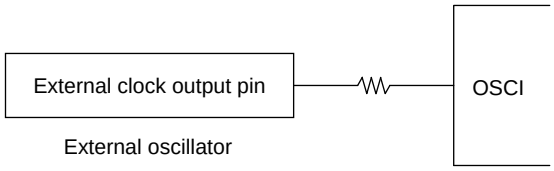
[Figure 7]

OSCI pin Peripheral Circuit

(1) Internal oscillator operating mode (Control data OC =“0”)
Connect OSCI pin to GND if internal oscillator operating mode is selected.

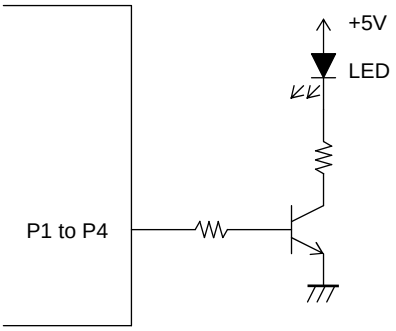


(2) External clock operating mode (Control data OC =“1”)
Input the external clock to OSCI pin if external clock operating mode is selected.



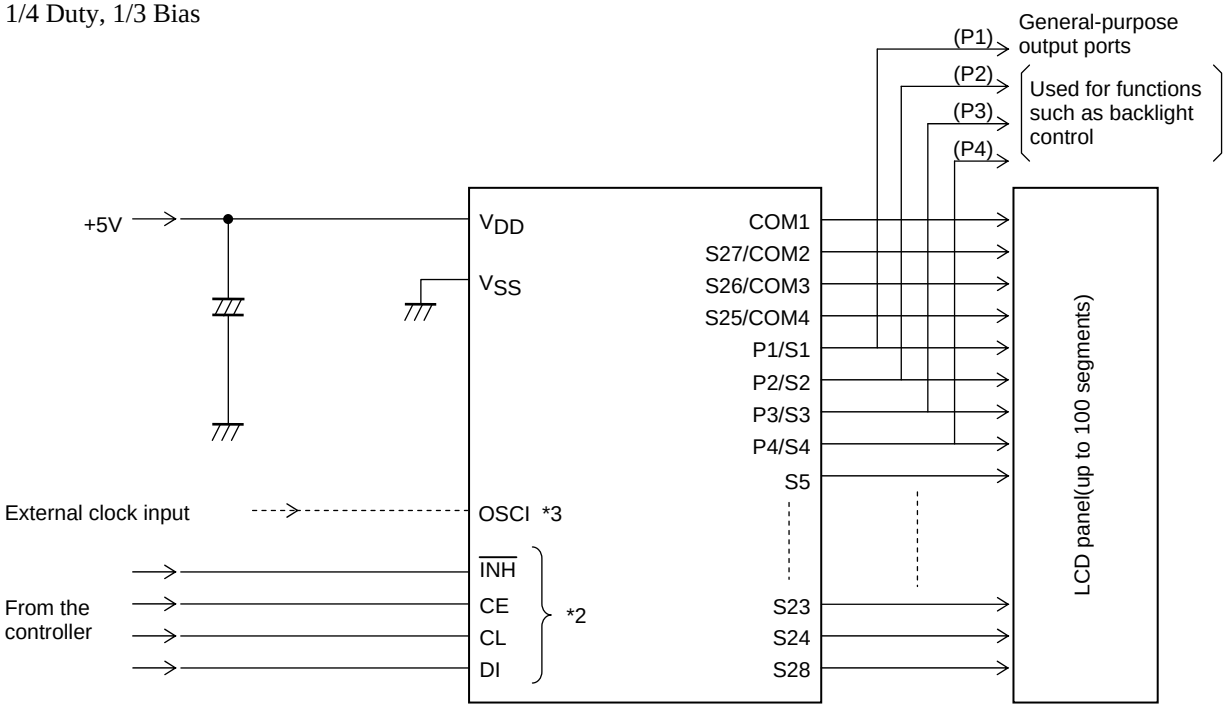
P1 to P4 pin Peripheral Circuit

It is recommended the circuit shown below be used to adjust the brightness of the LED backlight using the PWM output P1 to P4



Sample Applications Circuit 1

1/4 Duty, 1/3 Bias

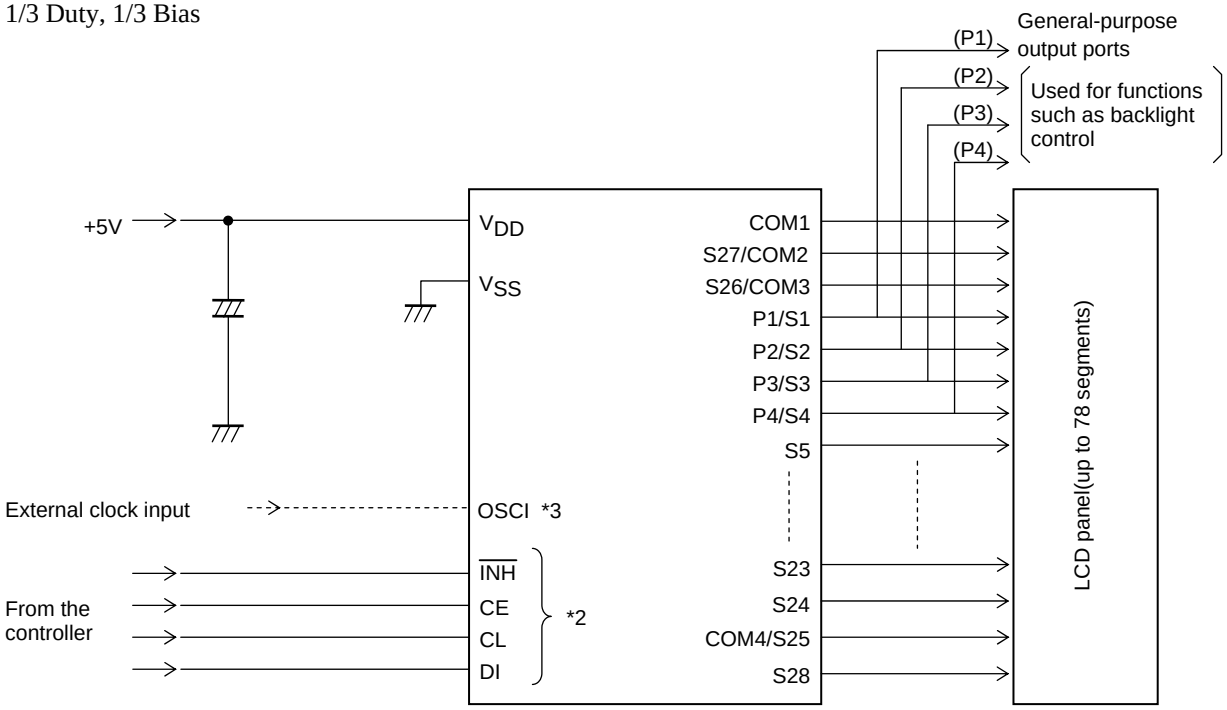


*2. The pins to be connected to the controller (CE, CL, DI, $\overline{INH}$) can handle 3.3V or 5V.

*3. External clock input pin OSCI is supported 3.3V or 5V. Connect to GND at internal oscillator operating mode, and input the external clock to OSCI pin at external clock operating mode.
(See "OSCI pin peripheral circuit")

Sample Application Circuit 2

1/3 Duty, 1/3 Bias

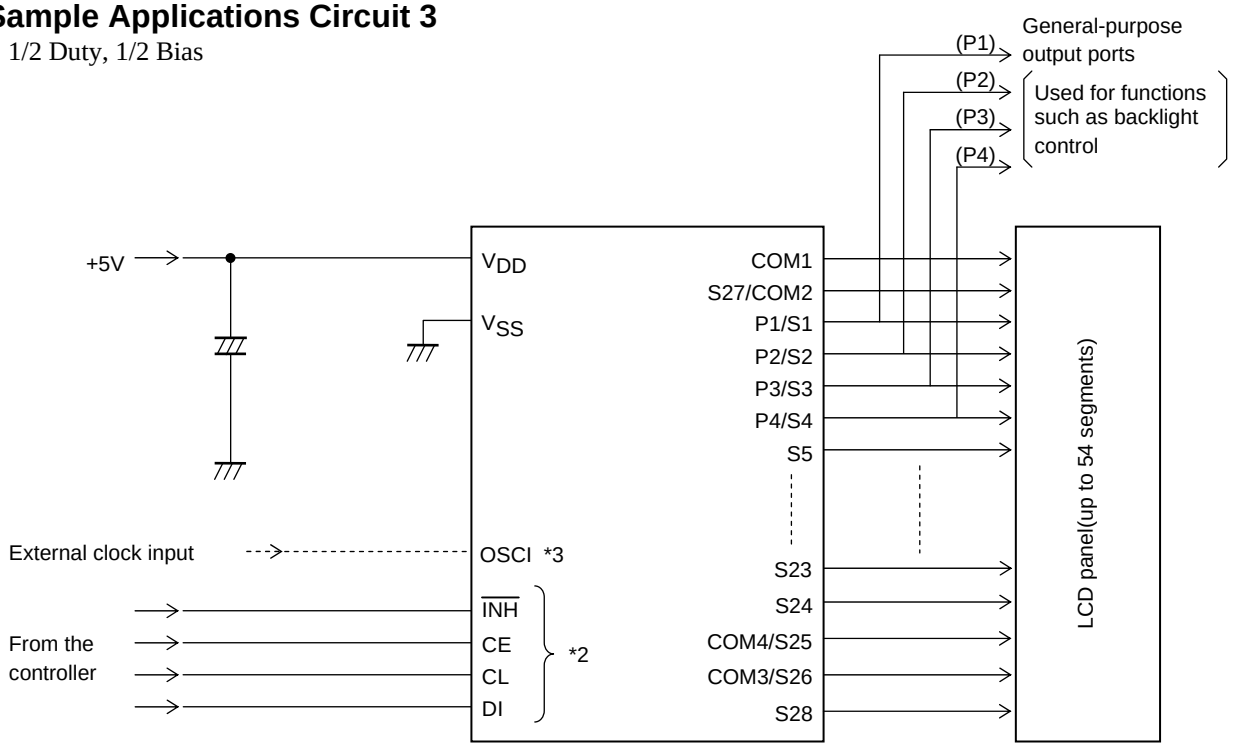


*2. The pins to be connected to the controller (CE, CL, DI, $\overline{INH}$) can handle 3.3V or 5V.

*3. External clock input pin OSCI is supported 3.3V or 5V. Connect to GND at internal oscillator operating mode, and input the external clock to OSCI pin at external clock operating mode.
(See "OSCI pin peripheral circuit")

Sample Applications Circuit 3

1/2 Duty, 1/2 Bias

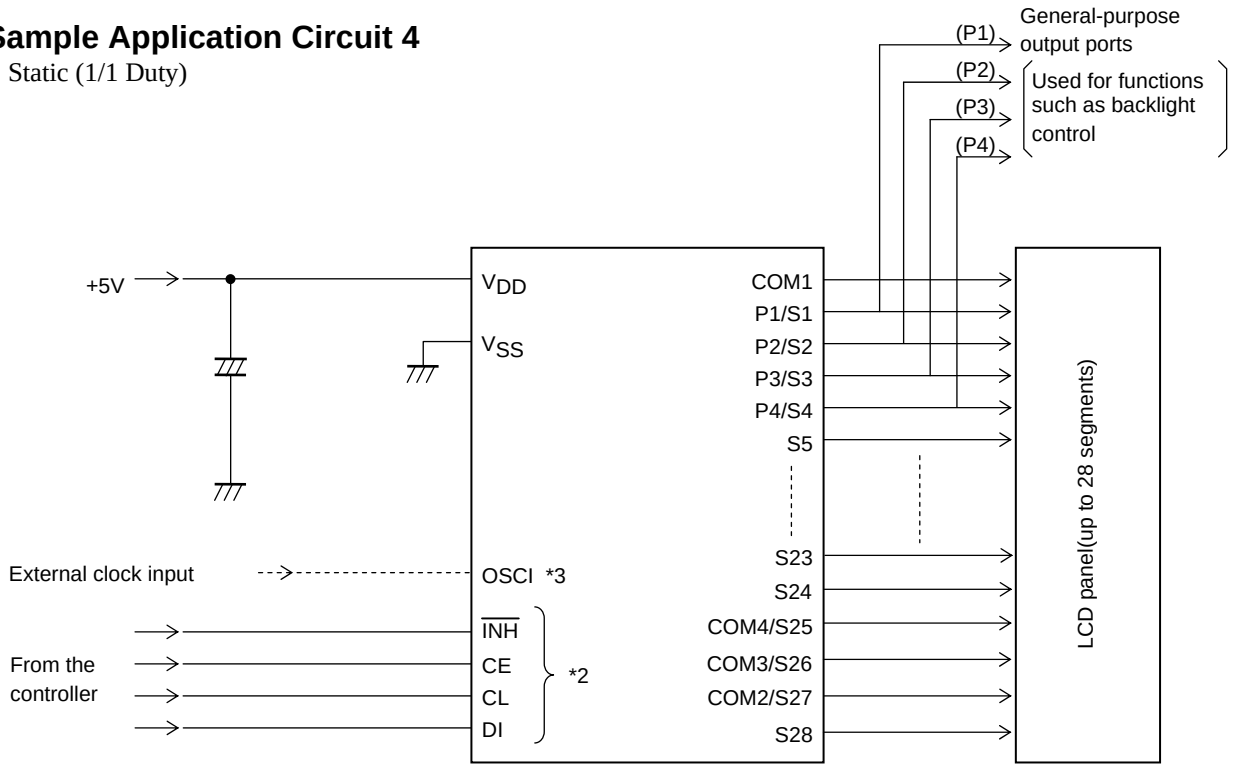


*2. The pins to be connected to the controller (CE, CL, DI, $\overline{INH}$) can handle 3.3V or 5V.

*3. External clock input pin OSCI is supported 3.3V or 5V. Connect to GND at internal oscillator operating mode, and input the external clock to OSCI pin at external clock operating mode.
(See "OSCI pin peripheral circuit")

Sample Application Circuit 4

Static (1/1 Duty)



*2. The pins to be connected to the controller (CE, CL, DI, $\overline{INH}$) can handle 3.3V or 5V.

*3. External clock input pin OSCI is supported 3.3V or 5V. Connect to GND at internal oscillator operating mode, and input the external clock to OSCI pin at external clock operating mode.
(See "OSCI pin peripheral circuit")

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC75843UGA-AH	TSSOP36(275mil) (Pb-Free / Halogen free)	1000 / Tape & Reel

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