# GaAs, pHEMT, MMIC, 0.25 W Power Amplifier, DC to 40 GHz

Data Sheet **HMC930A**

## FEATURES

**High output power for 1 dB compression (P1dB): 22 dBm**
**High saturated output power ($P_{SAT}$): 24 dBm**
**High gain: 13 dB**
**High output third-order intercept (IP3): 33.5 dBm**
**Supply voltage: 10 V at 175 mA**
**50 Ω matched input/output**
**Die size: 2.82 mm × 1.50 mm × 0.1 mm**

## APPLICATIONS

**Test instrumentation**
**Microwave radios and VSATs**
**Military and space**
**Telecommunications infrastructure**
**Fiber optics**

## FUNCTIONAL BLOCK DIAGRAM

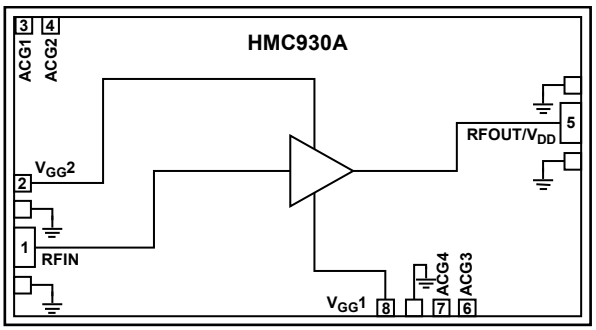


*Figure 1.*

## GENERAL DESCRIPTION

The HMC930A is a gallium arsenide (GaAs), pseudomorphic, high electron mobility transfer (pHEMT), monolithic microwave integrated circuit (MMIC), distributed power amplifier that operates from dc to 40 GHz. The HMC930A provides 13 dB of gain, 33.5 dBm output IP3, and 22 dBm of output power at 1 dB gain compression, requiring 175 mA from a 10 V supply. The HMC930A exhibits a slightly positive gain slope from 8 GHz to 32 GHz, making it ideal for electronic warfare (EW), electronic countermeasures (ECM), radar, and test equipment applications. The HMC930A amplifier inputs/outputs (I/Os) are internally matched to 50 Ω, facilitating integration into multichip modules (MCMs). All data is taken with the chip connected via two 0.025 mm (1 mil) wire bonds of minimal length at 0.31 mm (12 mils).

**Rev. 0** **Document Feedback**


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**www.analog.com**

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## REVISION HISTORY

**12/15—Revision 0: Initial Version**

# ELECTRICAL SPECIFICATIONS

## DC TO 12 GHz FREQUENCY RANGE

$T_A$ = 25°C, $V_{DD}$ = 10 V, $V_{GG}2$ = 3.5 V, $I_{DD}$ = 175 mA. Adjust $V_{GG}1$ between −2 V to 0 V to achieve $I_{DD}$ = 175 mA, typical.

**Table 1.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| FREQUENCY RANGE | | | DC | | 12 | GHz |
| GAIN | | | 11.5 | 13.5 | | dB |
| Gain Flatness | | | | ±0.5 | | dB |
| Gain Variation Over Temperature | | | | 0.01 | | dB/°C |
| RETURN LOSS | | | | | | |
| Input | | | | 18 | | dB |
| Output | | | | 28 | | dB |
| OUTPUT | | | | | | |
| Output Power for 1 dB Compression | P1dB | | 21 | 23 | | dBm |
| Saturated Output Power | $P_{SAT}$ | | | 25 | | dBm |
| Output Third-Order Intercept | IP3 | | | 36 | | dBm |
| NOISE FIGURE | | | | 4.5 | | dB |
| SUPPLY CURRENT | $I_{DD}$ | $V_{DD}$ = 10 V, $V_{GG}1$ = −0.8 V, typical | | 175 | | mA |

## 12 GHz TO 32 GHz FREQUENCY RANGE

$T_A$ = 25°C, $V_{DD}$ = 10 V, $V_{GG}2$ = 3.5 V, $I_{DD}$ = 175 mA. Adjust $V_{GG}1$ between −2 V to 0 V to achieve $I_{DD}$ = 175 mA, typical.

**Table 2.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| FREQUENCY RANGE | | | 12 | | 32 | GHz |
| GAIN | | | 11 | 13 | | dB |
| Gain Flatness | | | | ±0.3 | | dB |
| Gain Variation Over Temperature | | | | 0.017 | | dB/°C |
| RETURN LOSS | | | | | | |
| Input | | | | 16 | | dB |
| Output | | | | 20 | | dB |
| OUTPUT | | | | | | |
| Output Power for 1 dB Compression | P1dB | | | 22 | | dBm |
| Saturated Output Power | $P_{SAT}$ | | | 24 | | dBm |
| Output Third-Order Intercept | IP3 | | | 33.5 | | dBm |
| NOISE FIGURE | | | | 5 | | dB |
| SUPPLY CURRENT | $I_{DD}$ | $V_{DD}$ = 10 V, $V_{GG}1$ = −0.8 V, typical | | 175 | | mA |

## 32 GHz TO 40 GHz FREQUENCY RANGE

$T_A$ = 25°C, $V_{DD}$ = 10 V, $V_{GG}2$ = 3.5 V, $I_{DD}$ = 175 mA. Adjust $V_{GG}1$ between −2 V to 0 V to achieve $I_{DD}$ = 175 mA, typical.

**Table 3.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| FREQUENCY RANGE | | | 32 | | 40 | GHz |
| GAIN | | | 10 | 12 | | dB |
| Gain Flatness | | | | ±1.0 | | dB |
| Gain Variation Over Temperature | | | | 0.032 | | dB/°C |
| RETURN LOSS | | | | | | |
| Input | | | | 15 | | dB |
| Output | | | | 20 | | dB |
| OUTPUT | | | | | | |
| Output Power for 1 dB Compression | P1dB | | | 20 | | dBm |
| Saturated Output Power | $P_{SAT}$ | | | 23 | | dBm |
| Output Third-Order Intercept | IP3 | | | 29 | | dBm |
| NOISE FIGURE | | | | 7.5 | | dB |
| SUPPLY CURRENT | $I_{DD}$ | $V_{DD}$ = 10 V, $V_{GG}1$ = −0.8 V, typical | | 175 | | mA |

## TOTAL SUPPLY CURRENT BY $V_{DD}$

**Table 4.**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SUPPLY CURRENT | $I_{DD}$ | | | | |
| $V_{DD}$ = 9 V | | | 175 | | mA |
| $V_{DD}$ = 10 V | | | 175 | | mA |
| $V_{DD}$ = 11 V | | | 175 | | mA |

# ABSOLUTE MAXIMUM RATINGS

**Table 5.**

| Parameter | Rating |
|---|---|
| Drain Bias Voltage ($V_{DD}$) | 13 V |
| Gate Bias Voltage | |
| $V_{GG}1$ | −3 V to 0 V dc |
| $V_{GG}2$ | |
| $V_{DD}$ = 12 V | $V_{GG}2$ = 5.5 V, $I_{DD}$ >145 mA |
| $V_{DD}$ = 8.5 V to 11 V | $V_{GG}2$ = ($V_{DD}$ − 6.5 V) up to 4.5 V |
| $V_{DD}$ < 8.5 V | $V_{GG}2$ must remain > 2 V |
| RF Input Power (RFIN) | 22 dBm |
| Channel Temperature | 150°C |
| Continuous Power Dissipation, $P_{DISS}$ ($T_A$ = 85°C, Derate 69 mW/°C Above 85°C) | 2.1 W |
| Thermal Resistance (Channel to Die Bottom) | 31.1°C/W |
| Output Power into Voltage Standing Wave Ratio (VSWR) > 7:1 | 24 dBm |
| Storage Temperature Range | −65°C to +150°C |
| Operating Temperature Range | −55°C to +85°C |
| ESD Sensitivity, Human Body Model (HBM) | Class 1A, passed 250 V |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

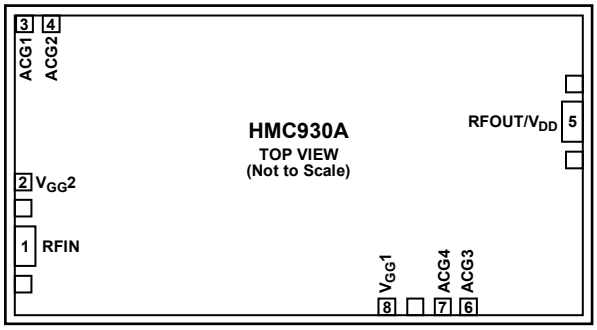


*Figure 2. Pad Configuration*

**Table 6. Pad Function Descriptions**

| Pad No. | Mnemonic | Description |
|---|---|---|
| 1 | RFIN | RF Input. This pin is dc-coupled and matched to 50 Ω. A blocking capacitor is required on this pin. |
| 2 | $V_{GG}2$ | Gate Control 2 for the Amplifier. Attach bypass capacitors as shown in Figure 37. For nominal operation, apply 3.5 V to $V_{GG}2$. |
| 3 | ACG1 | Low Frequency Termination 1. Attach bypass capacitors as shown in Figure 37. |
| 4 | ACG2 | Low Frequency Termination 2. Attach bypass capacitors as shown in Figure 37. |
| 5 | RFOUT/$V_{DD}$[1] | RF Output for the Amplifier (RFOUT). |
| | | DC Bias ($V_{DD}$). Connect $V_{DD}$ to the bias tee network to provide the drain current ($I_{DD}$). See Figure 37. |
| 6 | ACG3 | Low Frequency Termination 3. Attach bypass capacitors as shown in Figure 37. |
| 7 | ACG4 | Low Frequency Termination 4. Attach bypass capacitors as shown in Figure 37. |
| 8 | $V_{GG}1$ | Gate Control 1 for the Amplifier. Attach bypass capacitors as shown in Figure 37. Follow the procedures described in the Biasing Procedures section. |
| Die Bottom | GND | Die bottom must be connected to RF/dc ground. |

[1] RFOUT/$V_{DD}$ is a multifunction pad.

## INTERFACE SCHEMATICS

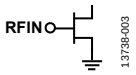


Figure 3. RFIN Interface Schematic

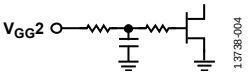


Figure 4. $V_{GG}2$ Interface Schematic

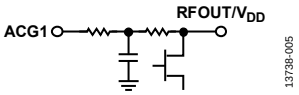


Figure 5. ACG1 and RFOUT/$V_{DD}$ Interface Schematic

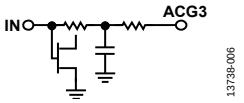


Figure 6. ACG3 Interface Schematic

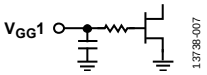


Figure 7. $V_{GG}1$ Interface Schematic


Figure 8. GND Interface Schematic

# TYPICAL PERFORMANCE CHARACTERISTICS

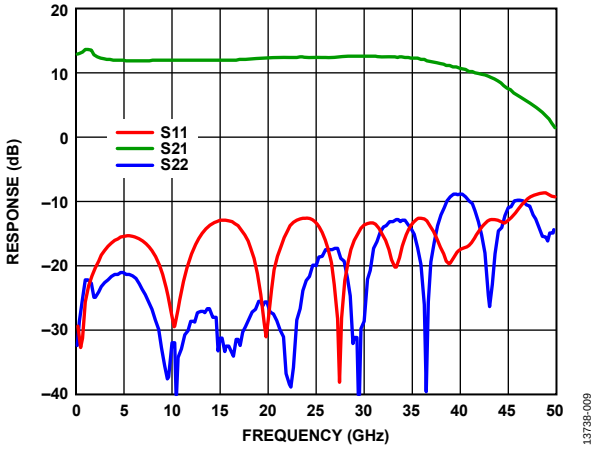


Figure 9. Gain and Return Loss

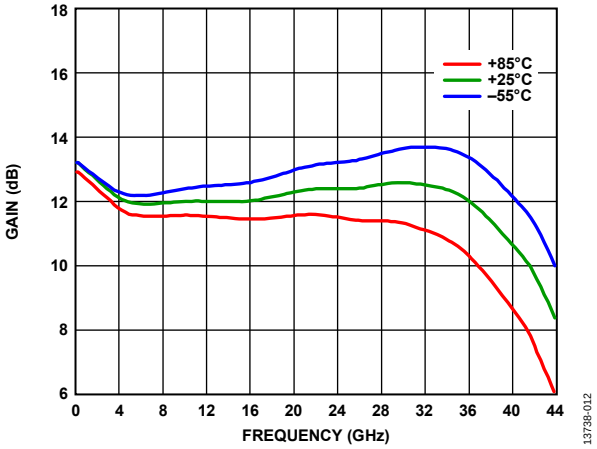


Figure 12. Gain vs. Frequency for Various Temperatures

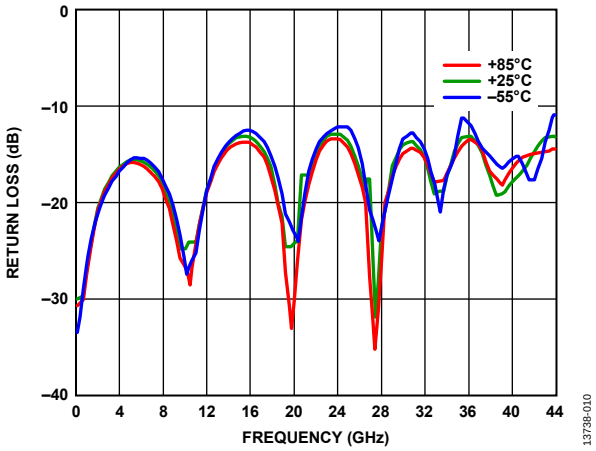


Figure 10. Input Return Loss vs. Frequency for Various Temperatures

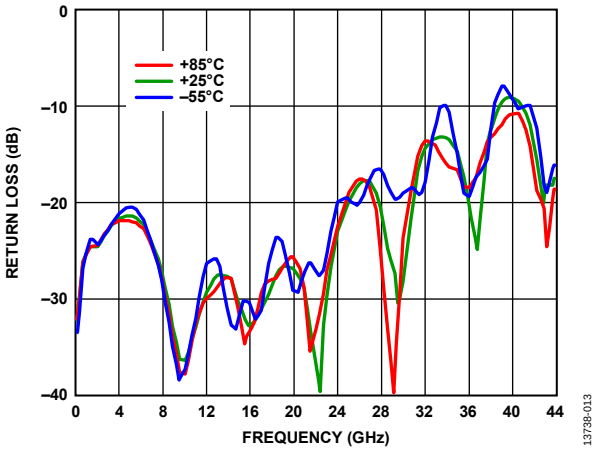


Figure 13. Output Return Loss vs. Frequency for Various Temperatures

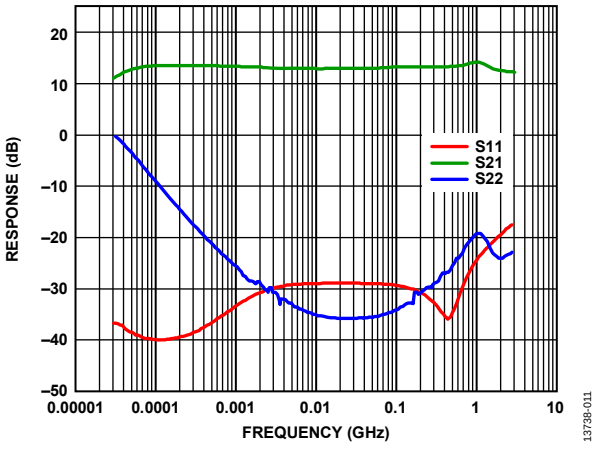


Figure 11. Low Frequency Gain and Return Loss

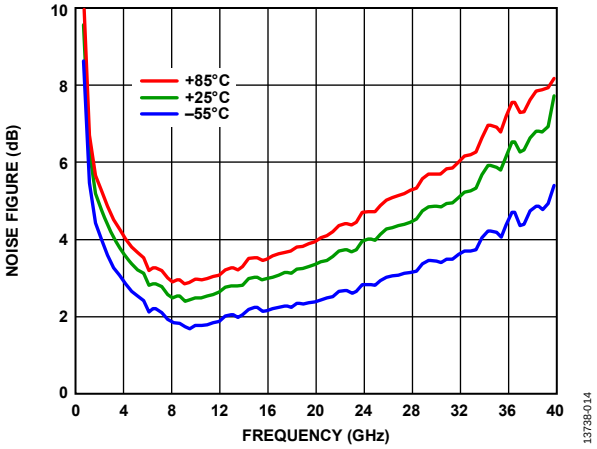


Figure 14. Noise Figure vs. Frequency for Various Temperatures

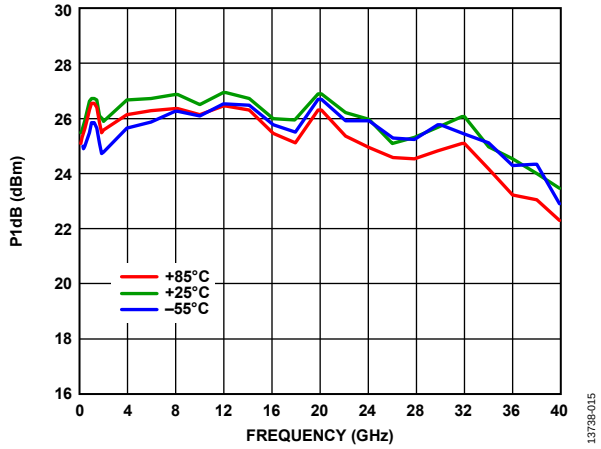


Figure 15. P1dB vs. Frequency for Various Temperatures

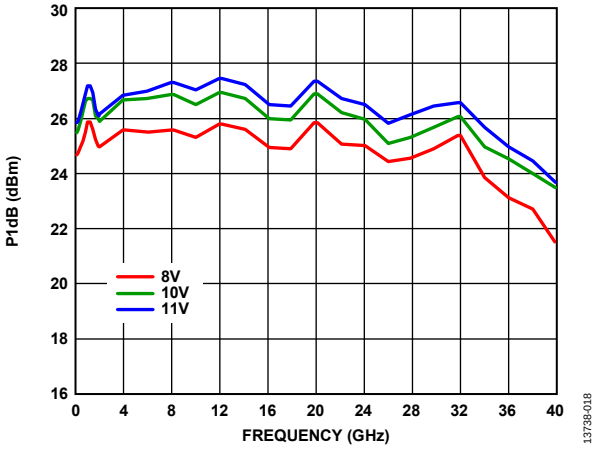


Figure 18. P1dB vs. Frequency for Various Supply Voltages

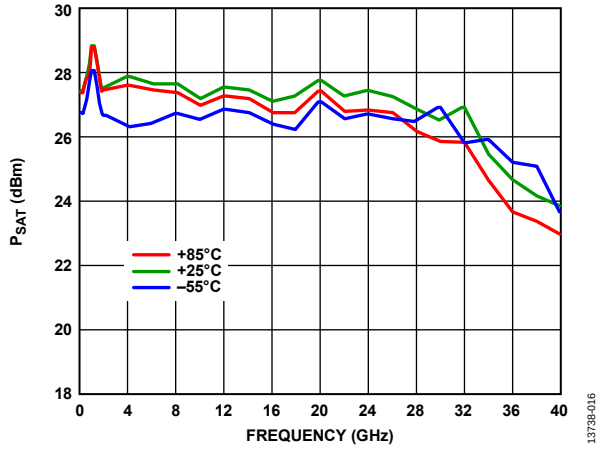


Figure 16. $P_{SAT}$ vs. Frequency for Various Temperatures

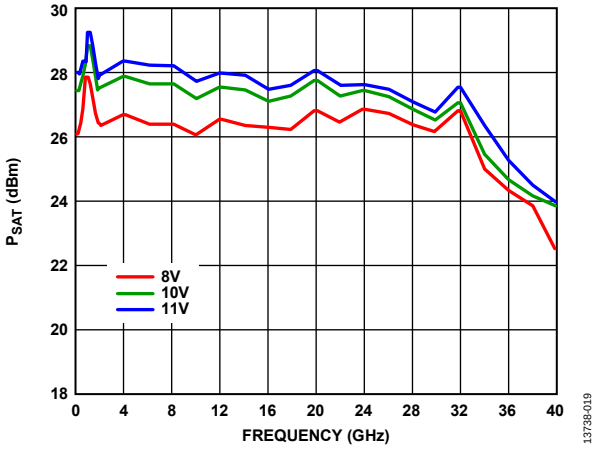


Figure 19. $P_{SAT}$ vs. Frequency for Various Supply Voltages

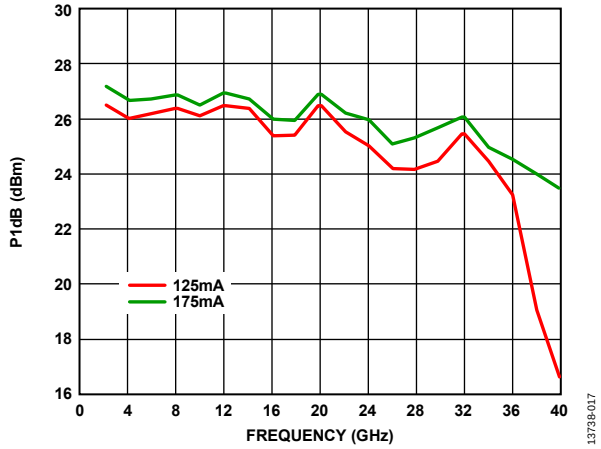


Figure 17. P1dB vs. Frequency and Supply Current

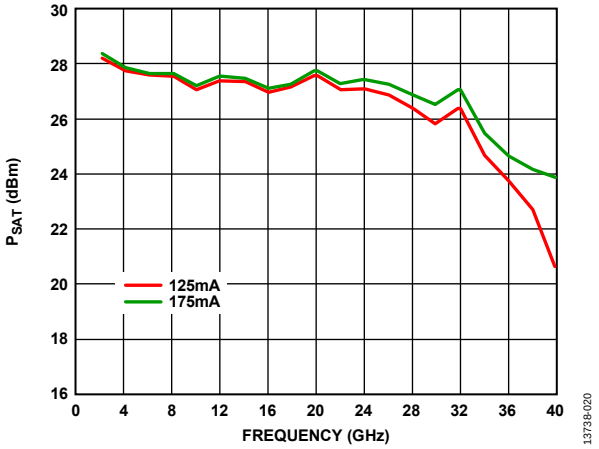


Figure 20. $P_{SAT}$ vs. Frequency and Supply Current

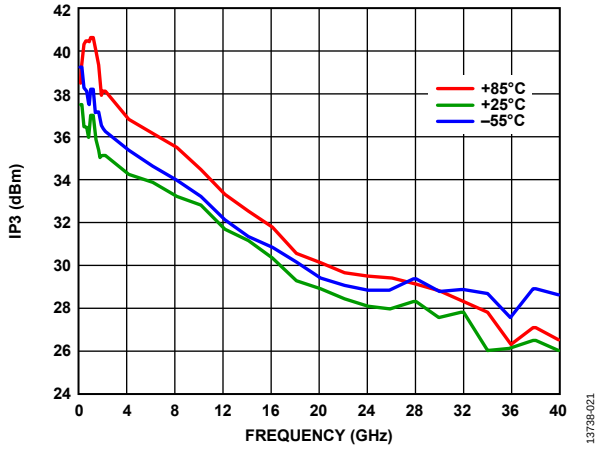


Figure 21. Output IP3 vs. Frequency for Various Temperatures at $P_{OUT}$ = 14 dBm/Tone

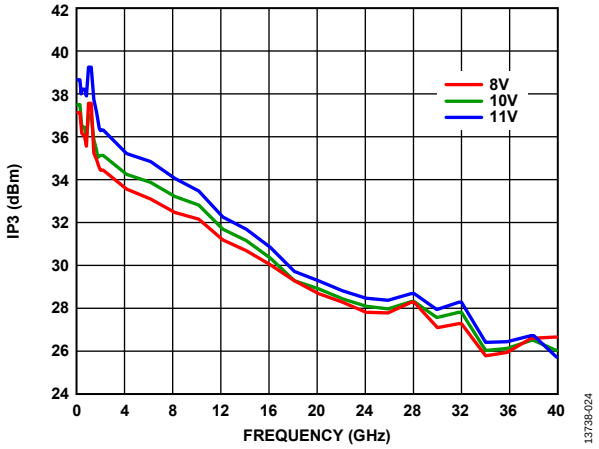


Figure 24. Output IP3 vs. Frequency for Various Supply Voltages at $P_{OUT}$ = 14 dBm/Tone

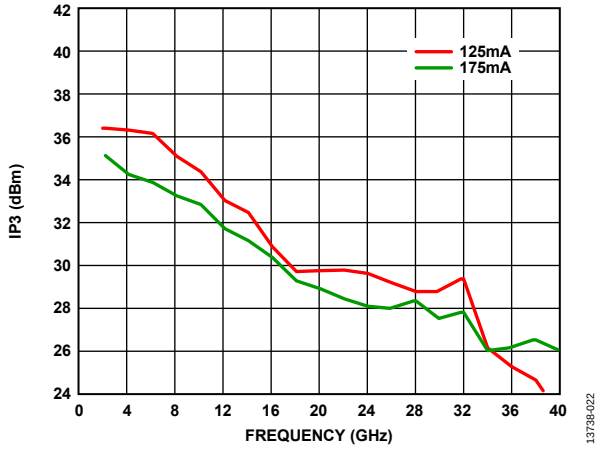


Figure 22. Output IP3 vs. Frequency and Supply Current at $P_{OUT}$ = 14 dBm/Tone

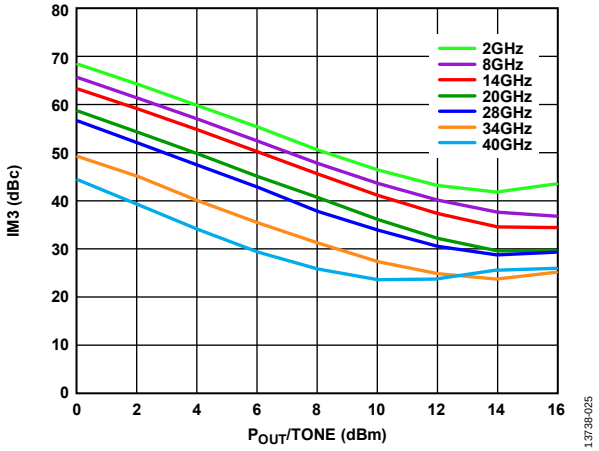


Figure 25. Output IM3 at $V_{DD}$ = 8 V

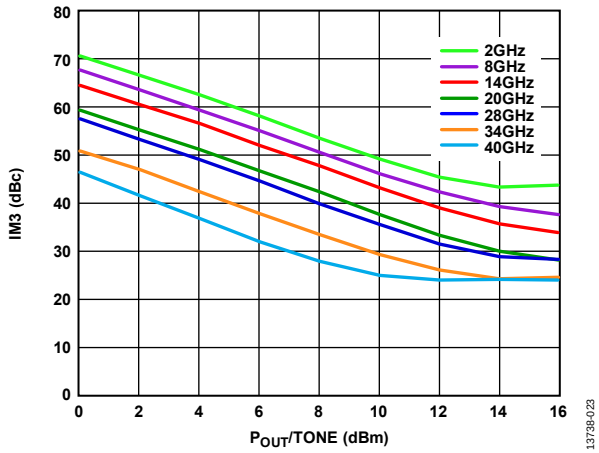


Figure 23. Output Third-Order Intermodulation Tone (IM3) at $V_{DD}$ = 10 V

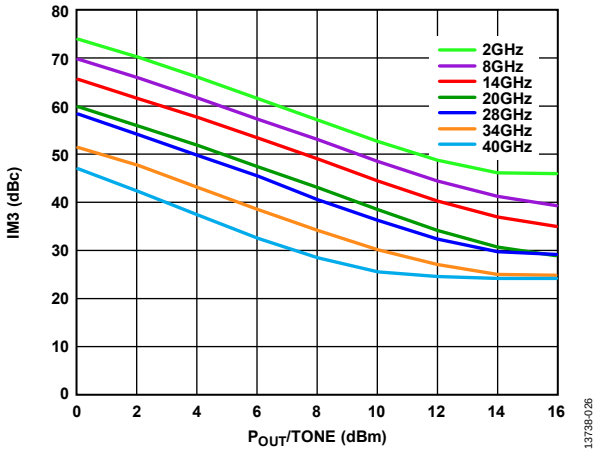


Figure 26. Output IM3 at $V_{DD}$ = 11 V

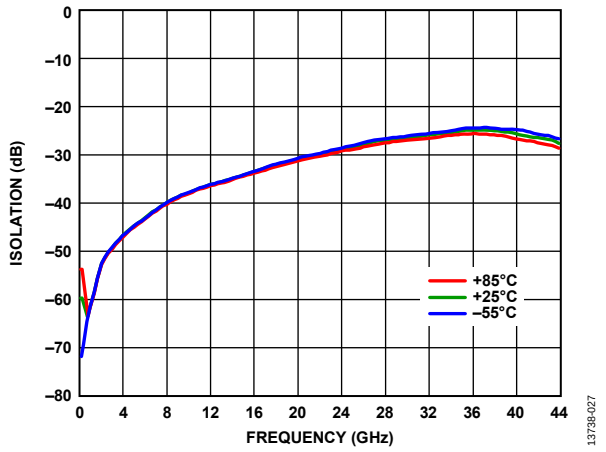


Figure 27. Reverse Isolation vs. Frequency for Various Temperatures

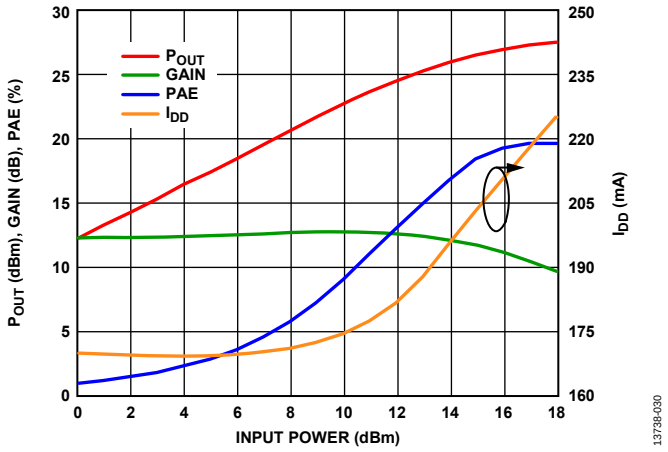


Figure 30. Power Compression at 20 GHz

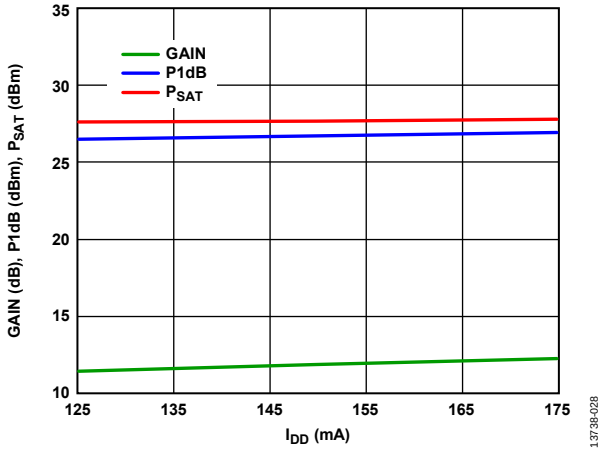


Figure 28. Gain and Power (P1dB and $P_{SAT}$) vs. Supply Current ($I_{DD}$) at 20 GHz

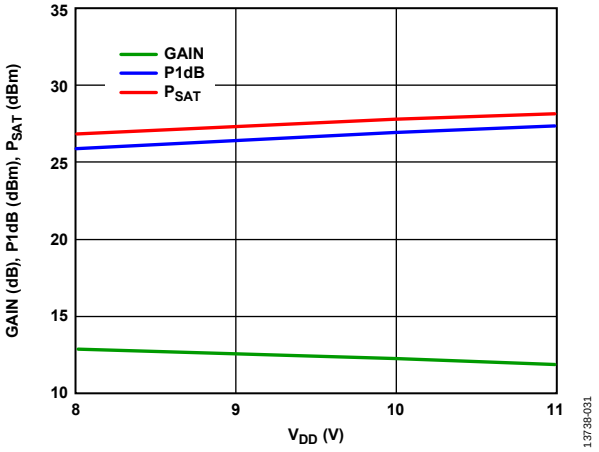


Figure 31. Gain and Power (P1dB and $P_{SAT}$) vs. Supply Voltage ($V_{DD}$) at 20 GHz

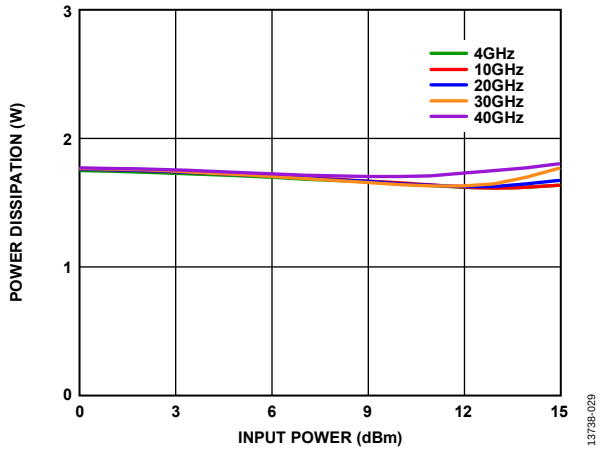


Figure 29. Power Dissipation

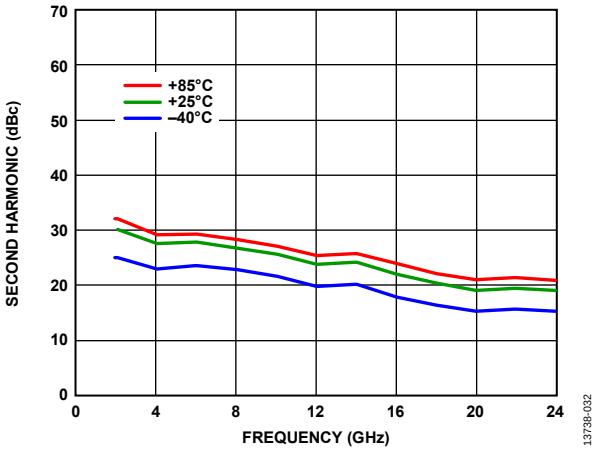


Figure 32. Second-Order Harmonic vs. Frequency for Various Temperatures at $P_{OUT}$ = 14 dBm, $V_{DD}$ = 10 V, $V_{GG}$ = 3.5 V, and $I_{DD}$ = 175 mA

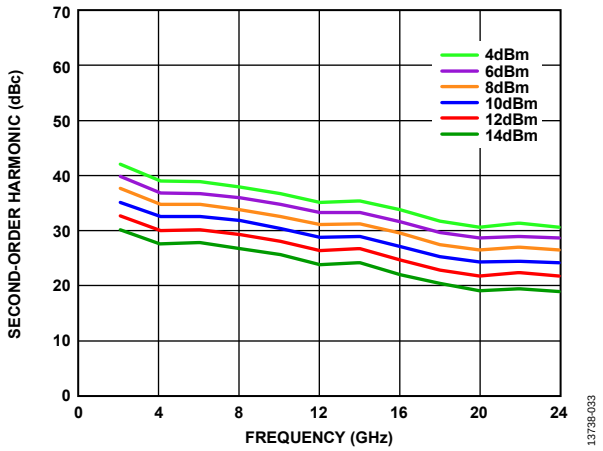


*Figure 33. Second-Order Harmonic vs. Frequency for Various $P_{OUT}$ Values, $V_{DD}$ = 10 V, $V_{GG}$ = 3.5 V, and $I_{DD}$ = 175 mA*

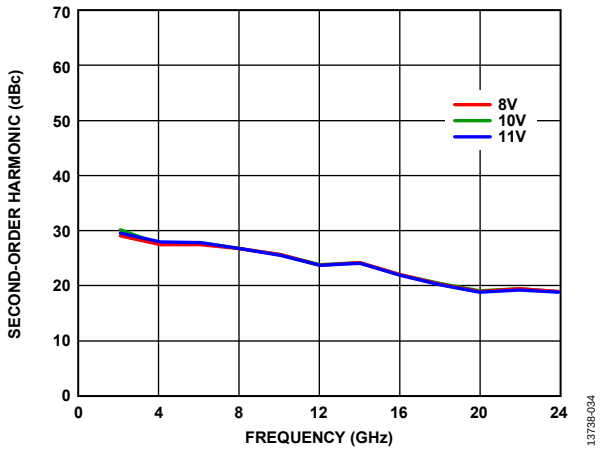


*Figure 34. Second-Order Harmonic vs. Frequency for Various $V_{DD}$ Values at $P_{OUT}$ = 14 dBm and $I_{DD}$ = 175 mA*

# THEORY OF OPERATION

The HMC930A is a GaAs, pHEMT, MMIC, cascaded, distributed power amplifier. The cascade distributed architecture uses a fundamental cell consisting of a stack of two field effect transistors (FETs) connected from source to drain. The basic schematic for a fundamental cell is shown in Figure 35. The fundamental cell is duplicated several times, with transmission lines connecting the drains of the top devices and the gates of the bottom devices, respectively. Additional circuit design techniques around each cell optimize the overall response. The major benefit of this architecture is that acceptable gain is maintained across a bandwidth that is far greater than what is typically provided by a single instance of the fundamental cell.

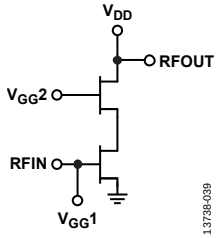


*Figure 35. Fundamental Cell Schematic*

To obtain the best performance from the HMC930A and to avoid damaging the device, follow the recommended biasing sequences described in the Biasing Procedures section.

# APPLICATIONS INFORMATION

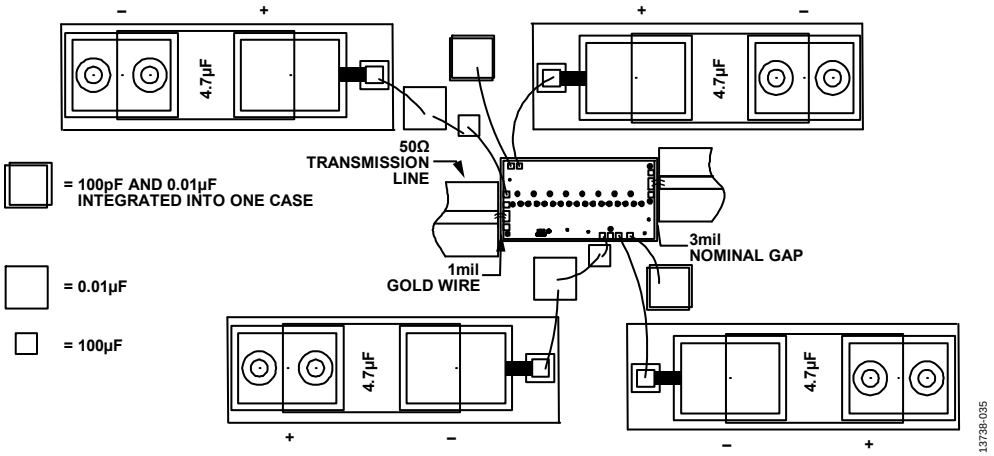


*Figure 36. Assembly Diagram*

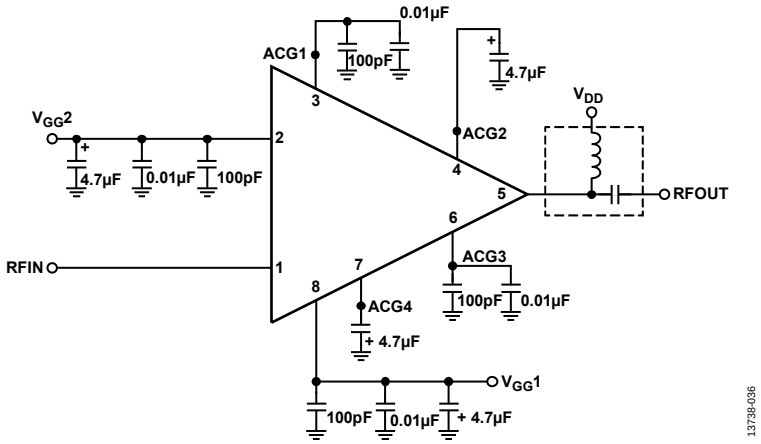


*Figure 37. Application Circuit*

## BIASING PROCEDURES

Capacitive bypassing is required for both $V_{GG}1$ and $V_{GG}2$, as shown in Figure 37. The capacitors to ground required for the ACG1 through ACG4 pads act as low frequency terminations; this helps flatten the overall frequency response by diminishing the gain at low frequencies.

The recommended biasing sequence during power-up is as follows:

1. Connect to GND.
2. Set $V_{GG}1$ to −2 V to pinch off the drain current.
3. Set $V_{DD}$ to 10 V (the drain current is pinched off).
4. Set $V_{GG}2$ to 3.5 V (the drain current is pinched off).
5. Adjust $V_{GG}1$ in a positive direction until a quiescent current ($I_{DD}$) of 175 mA is obtained.
6. Apply the RF signal.

The recommended biasing sequence during power-down is as follows:

1. Turn off the RF signal.
2. Set $V_{GG}1$ to −2 V to pinch off the drain current.
3. Set $V_{GG}2$ to 0 V.
4. Set $V_{DD}$ to 0 V.
5. Set $V_{GG}1$ to 0 V.

All measurements for the HMC930A are taken using the typical application circuit (see Figure 37) configured as shown Figure 36. The bias conditions shown in the Electrical Specifications section are the operating points recommended to optimize the overall performance. Unless otherwise noted, the data shown is taken using the recommended bias conditions. Operation of the HMC930A at different bias conditions may provide performance that differs from what is shown in the Typical Performance Characteristics section.

## MOUNTING AND BONDING TECHNIQUES FOR MILLIMETERWAVE GaAs MMICS

Attach the die directly to the ground plane eutectically or with conductive epoxy (see the Handling Precautions section, the Mounting section, and the Wire Bonding section).

Microstrip, 50 Ω, transmission lines on 0.127 mm (5 mil) thick alumina, thin film substrates are recommended for bringing the radio frequency to and from the chip (see Figure 38). When using 0.254 mm (10 mil) thick alumina thin film substrates, raise the die 0.150 mm (6 mils) to ensure that the surface of the die is coplanar with the surface of the substrate. One way to accomplish this is to attach the 0.102 mm (4 mil) thick die to a 0.150 mm (6 mil) thick, molybdenum (Mo) heat spreader (moly tab), which is then attached to the ground plane (see Figure 38).

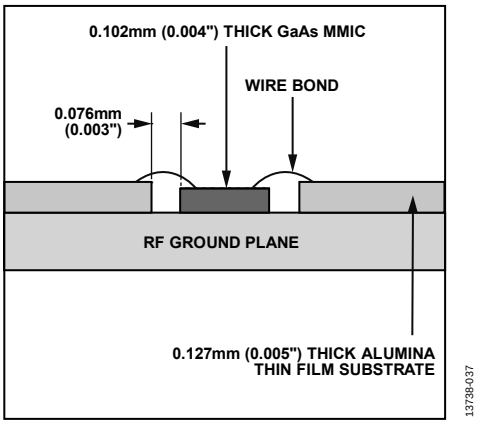


*Figure 38. Die Without the Moly Tab*

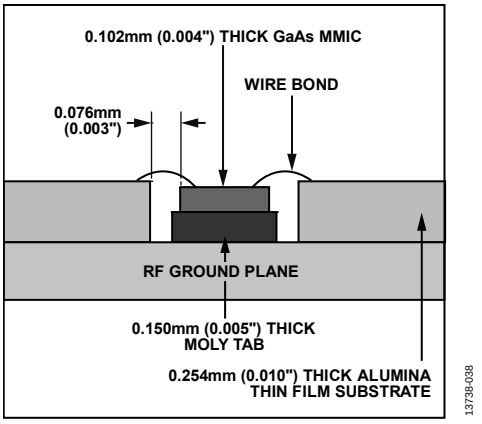


*Figure 39. Die With the Moly Tab*

Place microstrip substrates as close to the die as possible to minimize bond wire length. Typical die to substrate spacing is 0.076 mm to 0.152 mm (3 mil to 6 mil).

### *Handling Precautions*

To avoid permanent damage, follow these storage, cleanliness, static sensitivity, transient, and general handling precautions:

- Place all bare die in either waffle or gel-based ESD protective containers and then seal the die in an ESD protective bag for shipment. Once the sealed ESD protective bag is opened, store all die in a dry nitrogen environment.
- Handle the chips in a clean environment. Do not attempt to clean the chip using liquid cleaning systems.
- Follow ESD precautions to protect against ESD strikes.
- While bias is applied, suppress instrument and bias supply transients. Use shielded signal and bias cables to minimize inductive pick up.
- Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers. The surface of the chip may have fragile air bridges and must not be touched with vacuum collet, tweezers, or fingers.

### *Mounting*

The chip is back metallized and can be die mounted with AuSn eutectic preforms or with electrically conductive epoxy. Ensure that the mounting surface is clean and flat.

When attaching eutectic die, an 80/20 gold tin preform is recommended with a work surface temperature of 255°C and a tool temperature of 265°C. When hot 90/10 nitrogen/hydrogen gas is applied, ensure that tool tip temperature is 290°C. Do not expose the chip to a temperature greater than 320°C for more than 20 seconds. For attachment, no more than 3 seconds of scrubbing is required.

When attaching epoxy die, apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip once it is placed into position. Cure epoxy per the schedule of the manufacturer.

### *Wire Bonding*

RF bonds made with two 1 mil wires are recommended. Ensure that these bonds are thermosonically bonded with a force of 40 grams to 60 grams. DC bonds of a 0.001" (0.025 mm) diameter, thermosonically bonded, are recommended. Make ball bonds with a force of 40 grams to 50 grams and wedge bonds with a force of 18 grams to 22 grams. Make all bonds with a nominal stage temperature of 150°C. Apply a minimum amount of ultrasonic energy to achieve reliable bonds. Make all bonds as short as possible, less than 12 mils (0.31 mm).

# OUTLINE DIMENSIONS

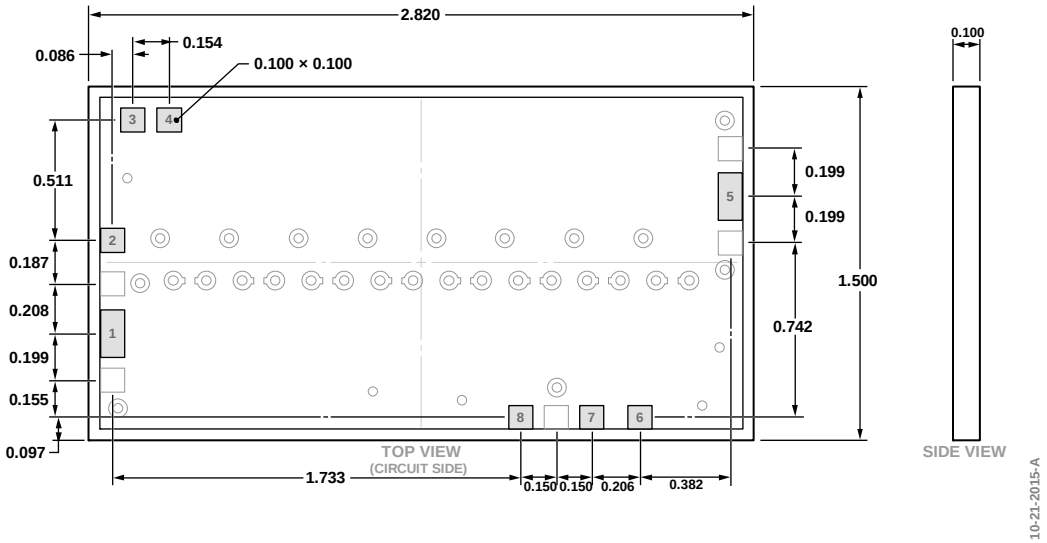


*Figure 40. 8-Pad Bare Die [CHIP]*
*(C-8-6)*
*Dimensions shown in millimeter*

## DIE PACKAGING INFORMATION

| Standard | Alternate Packaging |
|---|---|
| GP-2 (Gel Pack) | For alternate packaging information, contact Analog Devices, Inc. |

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| HMC930A | −55°C to +85°C | 8-Pad Bare Die [CHIP] | C-8-6 |