# 3A, 18V, 650kHz ACOT™ Synchronous Step-Down Converter

## General Description

The RT2858B is a synchronous DC/DC step-down converter with Advanced Constant On-Time (ACOT™) mode control. It achieves high power density to deliver up to 3A output current from a 4.5V to 18V input supply. The proprietary ACOT™ mode offers an optimal transient response over a wide range of loads and all kinds of ceramic capacitors, which allows the device to adopt very low ESR output capacitors for ensuring performance stabilization. In addition, the RT2858B keeps an excellent constant switching frequency under line and load variation and the integrated synchronous power switches with the ACOT™ mode operation provides high efficiency in whole output current load range. Cycle-by-cycle current limit provides an accurate protection by a valley detection of low-side MOSFET and external soft-start setting eliminates input current surge during startup. Protection functions also include output under voltage protection and thermal shutdown.

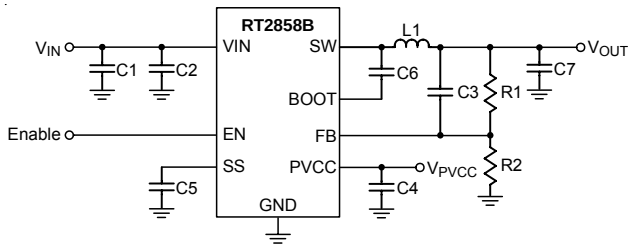
## Features

- **ACOT™ Control for Fast Transient, $f_{SW}$ Stability, and Robust Loop Stability with all-MLCC $C_{OUT}$**
- **4.5V to 18V Input Voltage Range**
- **3A Output Current**
- **$R_{DSON}$ 120mΩ/50mΩ for High Efficiency Across $I_{OUT}$ Range and Competitive Advantage for $I_{OUT}$ > 1.5A**
- **Advanced Constant On-Time Control**
- **Support All Ceramic Capacitors**
- **Up to 95% Efficiency**
- **650kHz $f_{SW}$; Start-Up into Pre-Biased Load; Adjustable Soft-Start; Internal Bootstrap**
- **Adjustable Output Voltage from 0.765V to 8V**
- **Enable; UVLO; OCP (Cycle-by-Cycle); and OTP (150°C)**
- **RoHS Compliant and Halogen Free**

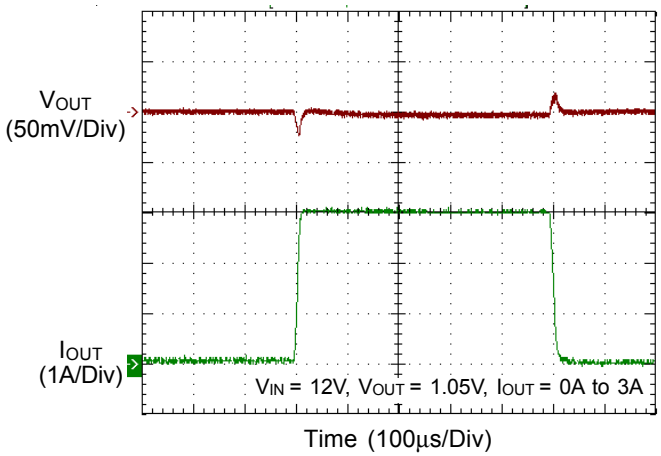
## Applications

- Industrial and Commercial Low Power Systems
- Computer Peripherals
- LCD Monitors and TVs
- Green Electronics/Appliances
- Point of Load Regulation for High-Performance DSPs, FPGAs, and ASICs

**Simplified Application Circuit**




**Load Transient Response**



## Ordering Information

RT2858B□□□

- Package Type
  SP : SOP-8 (Exposed Pad-Option 2)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- H : Hiccup Mode OVP and UVP
  N : OVP and UVP disable

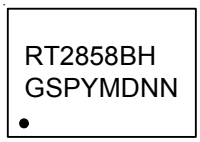
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

## Marking Information

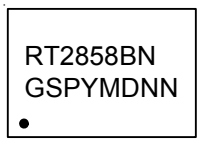
RT2858BHGSP




RT2858BHGSP : Product Number

YMDNN : Date Code

RT2858BNGSP

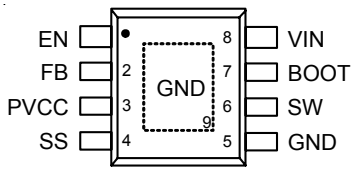



RT2858BNGSP : Product Number

YMDNN : Date Code

## Pin Configurations

(TOP VIEW)




SOP-8 (Exposed Pad)

## Absolute Maximum Ratings (Note 1)

- Supply Voltage, VIN ---------- –0.3V to 21V
- Switch Voltage, SW ---------- –0.8V to ($V_{IN}$ + 0.3V)
  <10ns ---------- –5V to 25V
- BOOT to SW ---------- –0.3V to 6V
- PVCC to VIN ---------- –18V to 0.3V
- Other Pins ---------- –0.3V to 21V
- Power Dissipation, $P_D$ @ $T_A$ = 25°C
  SOP-8 (Exposed Pad) ---------- 2.041W
- Package Thermal Resistance (Note 2)
  SOP-8 (Exposed Pad), $\theta_{JA}$ ---------- 49°C/W
  SOP-8 (Exposed Pad), $\theta_{JC}$ ---------- 8°C/W
- Junction Temperature Range ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

## Recommended Operating Conditions (Note 4)

- Supply Voltage, VIN ---------- 4.5V to 18V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

## Electrical Characteristics

($V_{IN}$ = 12V, $T_A$ = –40°C to 85°C, unless otherwise specified)

| Parameter | | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Supply Current** | | | | | | | |
| Shutdown Current | | $I_{SHDN}$ | EN = 0V, $T_A$ = 25°C | -- | 1 | 10 | μA |
| Quiescent Current | | $I_Q$ | EN = 5V, $V_{FB}$ = 0.8V, $T_A$ = 25°C | -- | 1 | 1.3 | mA |
| **Logic Threshold** | | | | | | | |
| EN Input Voltage | Logic-High | | | 2 | -- | 18 | V |
| | Logic-Low | | | -- | -- | 0.4 | |
| **$V_{FB}$ Voltage and Discharge Resistance** | | | | | | | |
| Feedback Threshold Voltage | | $V_{FB}$ | $T_A$ = 25°C | 0.757 | 0.765 | 0.773 | V |
| Feedback Input Current | | $I_{FB}$ | $V_{FB}$ = 0.8V, $T_A$ = 25°C | –0.1 | 0 | 0.1 | μA |
| **$V_{PVCC}$ Output** | | | | | | | |
| $V_{PVCC}$ Output Voltage | | $V_{PVCC}$ | 6V ≤ $V_{IN}$ ≤ 18V, 0 < $I_{PVCC}$ < 5mA, $T_A$ = 25°C | 4.8 | 5.1 | 5.4 | V |
| Line Regulation | | | 6V ≤ $V_{IN}$ ≤ 18V, $I_{PVCC}$ = 5mA | -- | -- | 20 | mV |
| Load Regulation | | | 0 < $I_{PVCC}$ < 5mA | -- | -- | 100 | mV |
| Output Current | | $I_{PVCC}$ | $V_{IN}$ = 6V, $V_{PVCC}$ = 4V, $T_A$ = 25°C | -- | 70 | -- | mA |

| Parameter | | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **$R_{DS(ON)}$** | | | | | | | |
| Switch-On Resistance | High-Side | $R_{DS(ON)\_H}$ | $V_{BOOT}$ – SW = 5V, $T_A$ = 25°C | -- | 120 | -- | mΩ |
| | Low-Side | $R_{DS(ON)\_L}$ | $T_A$ = 25°C | -- | 50 | -- | |
| **Current Limit** | | | | | | | |
| Current Limit | | $I_{LIM}$ | | 4 | 5 | 6 | A |
| **Thermal Shutdown** | | | | | | | |
| Thermal Shutdown Threshold | | $T_{SD}$ | | -- | 150 | -- | °C |
| Thermal Shutdown Hysteresis | | $\Delta T_{SD}$ | | -- | 20 | -- | °C |
| **On-Time Timer Control** | | | | | | | |
| On-Time | | $t_{ON}$ | $V_{IN}$ = 12V, $V_{OUT}$ = 1.05V | -- | 135 | -- | ns |
| Minimum Off-Time | | $t_{OFF(MIN)}$ | $V_{FB}$ = 0.7V, $T_A$ = 25°C | -- | 260 | 310 | ns |
| **Soft-Start** | | | | | | | |
| SS Charge Current | | | $V_{SS}$ = 0V | 1.4 | 2 | 2.6 | μA |
| SS Discharge Current | | | $V_{SS}$ = 0.5V | 0.1 | 0.2 | -- | mA |
| **UVLO** | | | | | | | |
| UVLO Threshold | | | VIN Rising to Wake up $V_{PVCC}$ | 3.6 | 3.85 | 4.1 | V |
| Hysteresis | | | | 130 | 350 | 400 | mV |

**Note 1.** Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

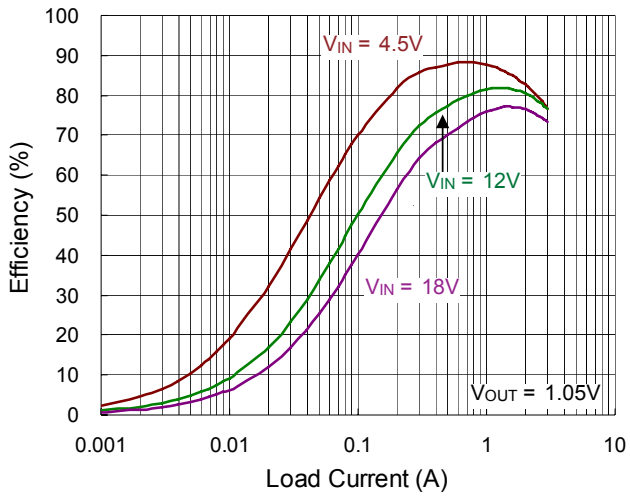
**Note 2.** $\theta_{JA}$ is measured at $T_A$ = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. $\theta_{JC}$ is measured at the exposed pad of the package. The PCB copper area with exposed pad is 70mm$^2$ (please see PCB Layout section for recommended shape & board physical design guidance).

**Note 3.** Devices are ESD sensitive. Handling precaution is recommended.

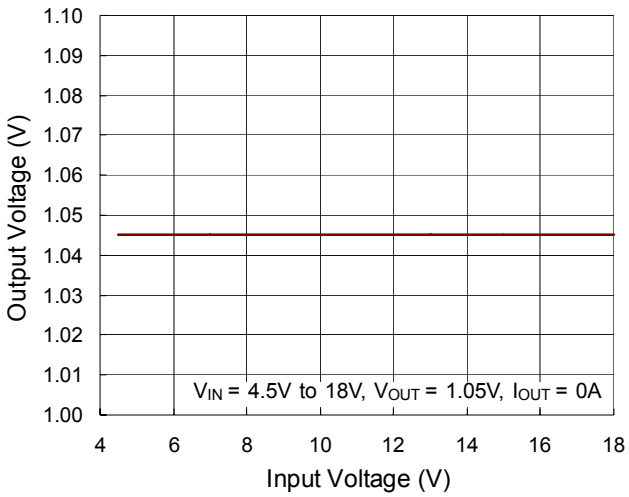
**Note 4.** The device is not guaranteed to function outside its operating conditions.

## Typical Operating Characteristics

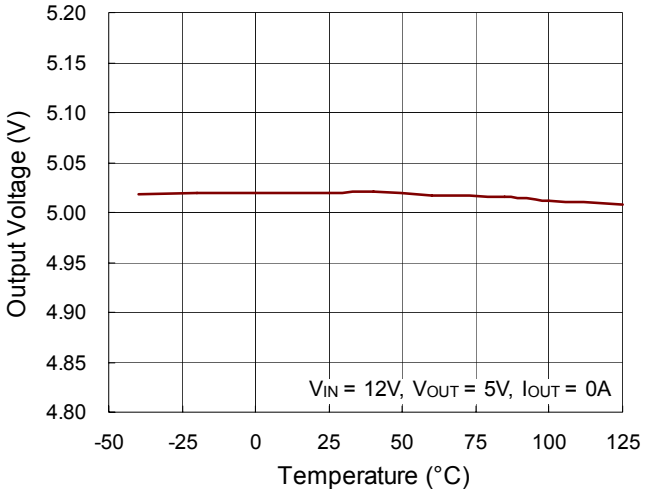
### Efficiency vs. Load Current



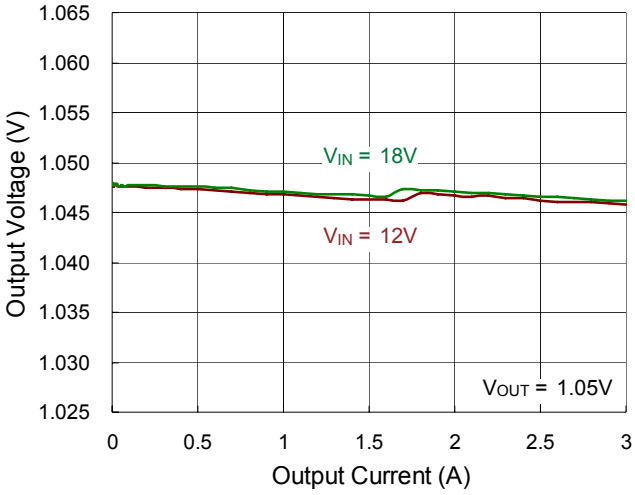

### Output Voltage vs. Input Voltage



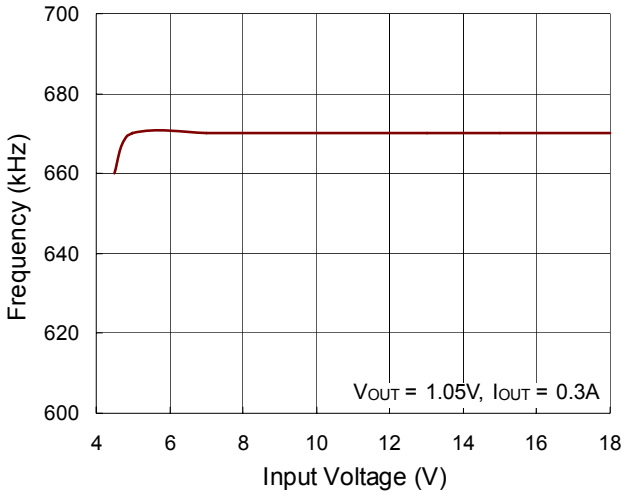

### Output Voltage vs. Temperature



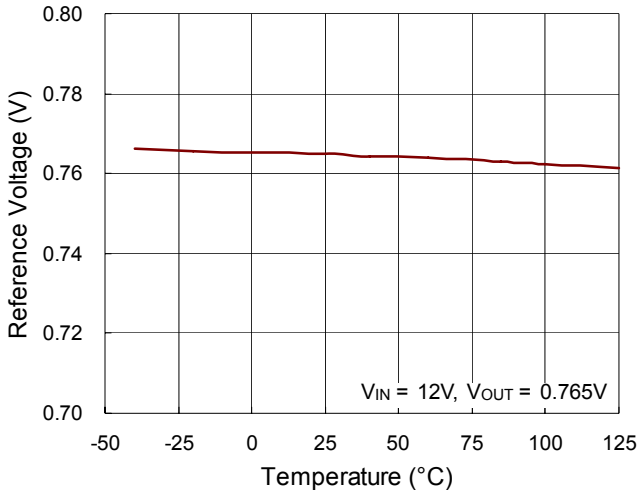

### Output Voltage vs. Output Current



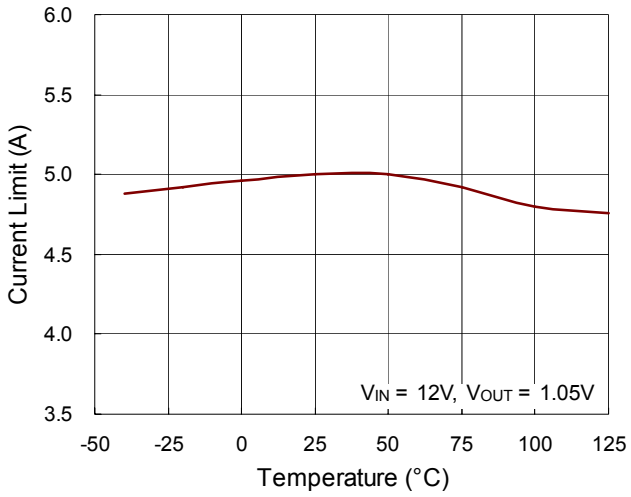

### Frequency vs. Input Voltage



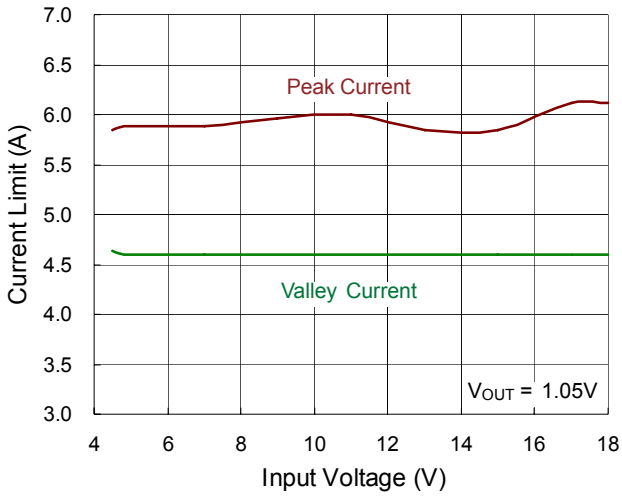

### Reference Voltage vs. Temperature



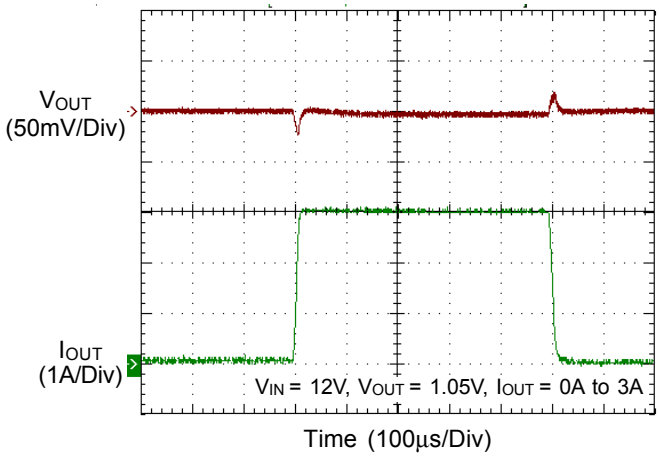
### Current Limit vs. Temperature



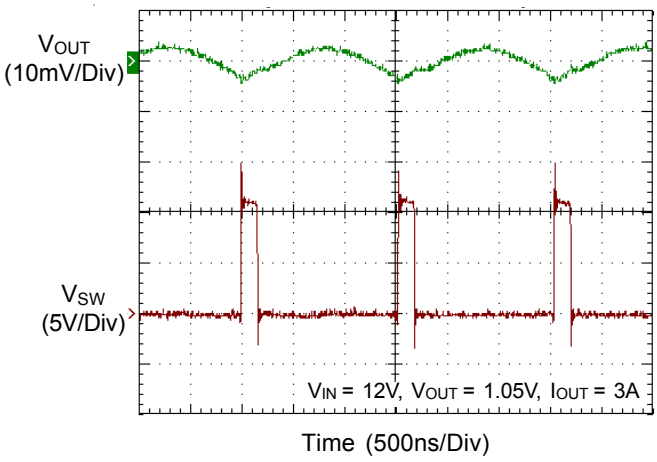

### Current Limit vs. Input Voltage



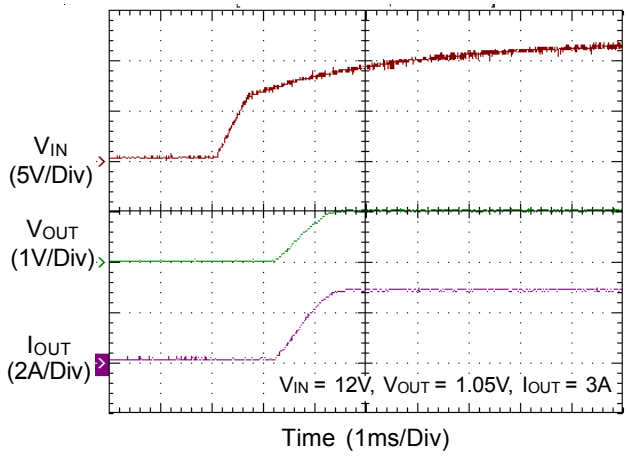

### Load Transient Response



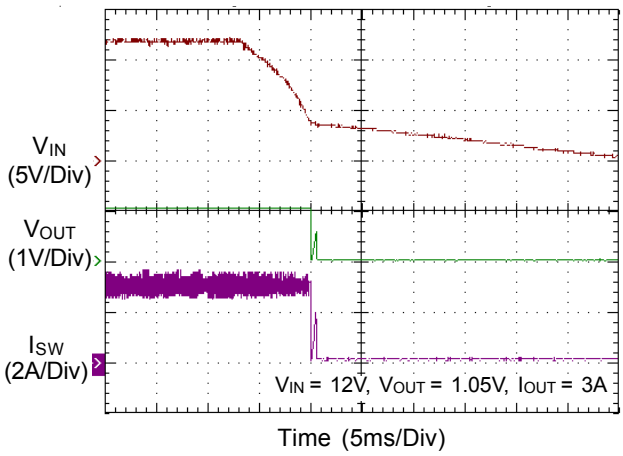

### VOUT Ripple



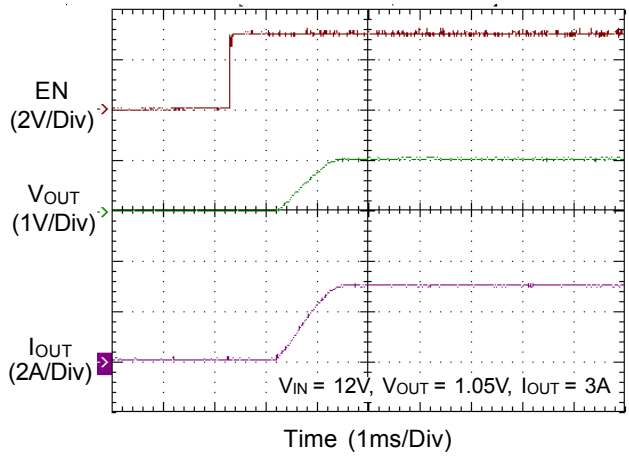

### Power On from VIN



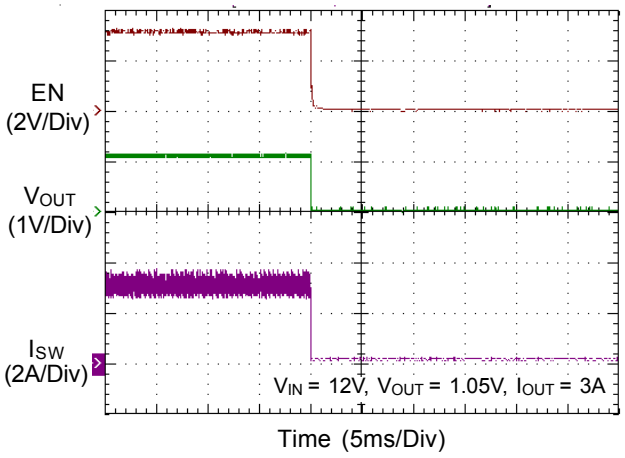

### Power Off from VIN



**Power On from EN**



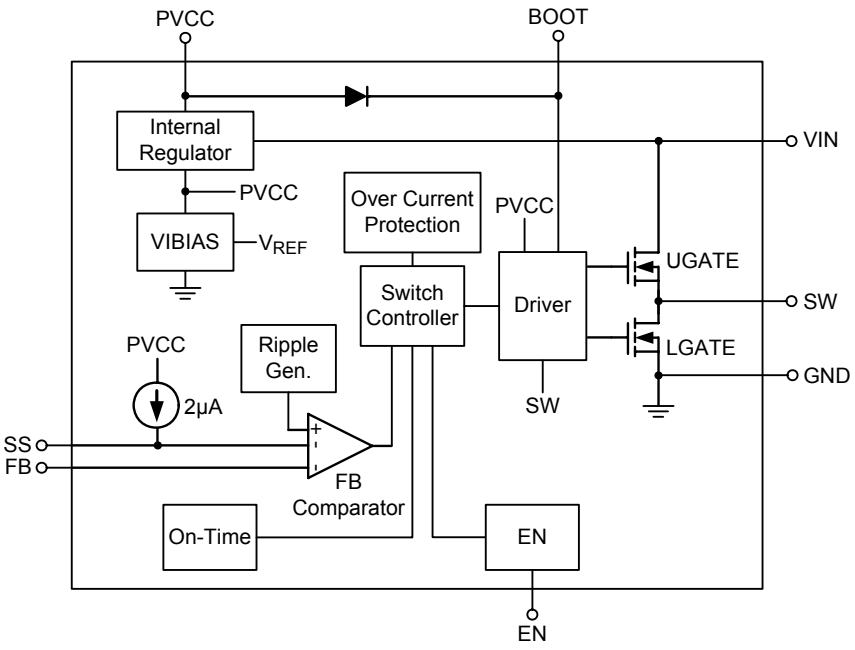

**Power Off from EN**



## Functional Pin Description

| Pin No. | Pin Name | Pin Function |
|---|---|---|
| 1 | EN | Enable Control Input. A logic-high enables the converter; a logic-low forces the IC into shutdown mode reducing the supply current to less than 10μA. |
| 2 | FB | Feedback Voltage Input. It is used to regulate the output of the converter to a set value via an external resistive voltage divider. The feedback threshold voltage is 0.765V typically. |
| 3 | PVCC | Regulator Output for Internal Circuit. Connect a 1μF capacitor to GND to stabilize output voltage. |
| 4 | SS | Soft-Start Time Setting. SS controls the soft-start period. Connect a capacitor from SS to GND to set the soft-start period. A 3.9nF capacitor sets the soft-start period of $V_{OUT}$ to 2.6ms. |
| 5, 9 (Exposed Pad) | GND | Ground. The Exposed pad should be soldered to a large PCB and connected to GND for maximum thermal dissipation. |
| 6 | SW | Switch Node. Connect this pin to an external L-C filter. |
| 7 | BOOT | Bootstrap Supply for High-Side Gate Driver. Connect a 0.1μF or greater ceramic capacitor between the BOOT to SW pins. |
| 8 | VIN | Power Input. The input voltage range is from 4.5V to 18V. Must bypass with a suitably large ( ≥10μF x 2) ceramic capacitor. |

## Function Block Diagram



## Operation

In normal operation, the high-side N-MOSFET is turned on when the FB Comparator sets the Switch Controller, and it is turned off when On-Time Controller resets the Switch Controller. While the high-side N-MOSFET is turned off, the low-side N-MOSFET is turned on and waits for the FB Comparator to set the beginning of next cycle.

The FB Comparator sets the Switch Controller by comparing the feedback signal (FB) from output voltage with the internal 0.765V reference. When load transient induces VOUT drop, the FB voltage will be less than its threshold voltage. This means that the high-side N-MOSFET will turn on again immediately after minimum off-time expired. The switching frequency will vary during the transient period thus can provide a very fast transient response. After the load transient finished, the RT2858B will be back to steady state with a constant switching frequency.

### Enable

Activate internal regulator once EN input level is higher than the target level. Force IC to enter shutdown mode when the EN input level is lower than 0.4V

### Internal Regulator

Provide internal power for logic control and switch gate drivers.

### On-Time Controller

Control on-time according to VIN and SW to obtain constant switching frequency.

### OVP/UVP Protection

The RT2858B detects over and under voltage conditions by monitoring the feedback voltage on FB pin. The two functions are enabled after approximately 1.7 times the soft-start time. When the feedback voltage becomes higher than 120% of the target voltage, the OVP comparator will go high to turn off both internal high side and low side MOSFETs. When the feedback voltage is lower than 70% of the target voltage for 250μs, the UVP comparator will go high to turn off both internal high side and low side MOSFETs.

## Typical Application Circuit

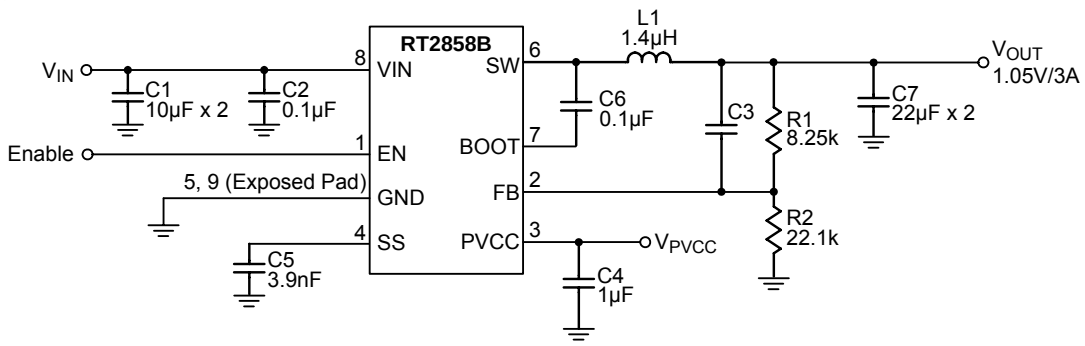



**Table 1. Suggested Component Values ($V_{IN}$ = 12V)**

| $V_{OUT}$ (V) | R1 (kΩ) | R2 (kΩ) | C3 (pF) | L1 (µH) | C7 (µF) |
|---|---|---|---|---|---|
| 1 | 6.81 | 22.1 | -- | 1.4 | 22 to 68 |
| 1.05 | 8.25 | 22.1 | -- | 1.4 | 22 to 68 |
| 1.2 | 12.7 | 22.1 | -- | 1.4 | 22 to 68 |
| 1.8 | 30.1 | 22.1 | 5 to 22 | 2 | 22 to 68 |
| 2.5 | 49.9 | 22.1 | 5 to 22 | 2 | 22 to 68 |
| 3.3 | 73.2 | 22.1 | 5 to 22 | 2 | 22 to 68 |
| 5 | 124 | 22.1 | 5 to 22 | 3.3 | 22 to 68 |
| 7 | 180 | 22.1 | 5 to 22 | 3.3 | 22 to 68 |

## Design Procedure

### Inductor Selection

Selecting an inductor involves specifying its inductance and also its required peak current. The exact inductor value is generally flexible and is ultimately chosen to obtain the best mix of cost, physical size, and circuit efficiency. Lower inductor values benefit from reduced size and cost and they can improve the circuit's transient response, but they increase the inductor ripple current and output voltage ripple and reduce the efficiency due to the resulting higher peak currents. Conversely, higher inductor values increase efficiency, but the inductor will either be physically larger or have higher resistance since more turns of wire are required and transient response will be slower since more time is required to change current (up or down) in the inductor. A good compromise between size, efficiency, and transient response is to use a ripple current ($\Delta I_L$) about 20-50% of the desired full output load current. Calculate the approximate inductor value by selecting the input and output voltages, the switching frequency ($f_{SW}$), the maximum output current ($I_{OUT(MAX)}$) and estimating a $\Delta I_L$ as some percentage of that current.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Once an inductor value is chosen, the ripple current ($\Delta I_L$) is calculated to determine the required peak inductor current.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L} \text{ and } I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

To guarantee the required output current, the inductor needs a saturation current rating and a thermal rating that exceeds $I_{L(PEAK)}$. These are minimum requirements. To maintain control of inductor current in overload and short-circuit conditions, some applications may desire current ratings up to the current limit value. However, the IC's output under-voltage shutdown feature make this unnecessary for most applications.

$I_{L(PEAK)}$ should not exceed the minimum value of IC's upper current limit level or the IC may not be able to meet the desired output current. If needed, reduce the inductor ripple current ($\Delta I_L$) to increase the average inductor current (and the output current) while ensuring that $I_{L(PEAK)}$ does not exceed the upper current limit level.

For best efficiency, choose an inductor with a low DC resistance that meets the cost and size requirements. For low inductor core losses some type of ferrite core is usually best and a shielded core type, although possibly larger or more expensive, will probably give fewer EMI and other noise problems.

Considering the Typical Operating Circuit for 1.05V output at 3A and an input voltage of 12V, using an inductor ripple of 1A (33%), the calculated inductance value is :

$$L = \frac{1.05V \times (12V - 1.05V)}{12V \times 650kHz \times 1A} = 1.47\mu H$$

The ripple current was selected at 1A and, as long as we use the calculated 1.47µH inductance, that should be the actual ripple current amount. Typically the exact calculated inductance is not readily available and a nearby value is chosen. In this case 1.4µH was available and actually used in the typical circuit. To illustrate the next calculation, assume that for some reason is was necessary to select a 1.8µH inductor (for example). We would then calculate the ripple current and required peak current as below :

$$\Delta I_L = \frac{1.05V \times (12V - 1.05V)}{12V \times 650kHz \times 1.8\mu H} = 0.82A$$

$$\text{and } I_{L(PEAK)} = 3A + \frac{0.82}{2} = 3.41A$$

For the 1.8µH value, the inductor's saturation and thermal rating should exceed 3.41A. Since the actual value used was 1.4µH and the ripple current exactly 1A, the required peak current is 3.53A.

### Input Capacitor Selection

The input filter capacitors are needed to smooth out the switched current drawn from the input power source and to reduce voltage ripple on the input. The actual capacitance value is less important than the RMS current rating (and voltage rating, of course). The RMS input ripple current ($I_{RMS}$) is a function of the input voltage, output voltage, and load current :

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT} \times (V_{VIN} - V_{OUT})}}{V_{VIN}}$$

Ceramic capacitors are most often used because of their low cost, small size, high RMS current ratings, and robust surge current capabilities. However, take care when these

capacitors are used at the input of circuits supplied by a wall adapter or other supply connected through long, thin wires. Current surges through the inductive wires can induce ringing at the RT2858B's input which could potentially cause large, damaging voltage spikes VIN. If this phenomenon is observed, some bulk input capacitance may be required. Ceramic capacitors (to meet the RMS current requirement) can be placed in parallel with other types such as tantalum, electrolytic, or polymer (to reduce ringing and overshoot).

Choose capacitors rated at higher temperatures than required. Several ceramic capacitors may be paralleled to meet the RMS current, size, and height requirements of the application. The typical operating circuit uses two 10μF and one 0.1μF low ESR ceramic capacitors on the input.

### Output Capacitor Selection

The RT2858B are optimized for ceramic output capacitors and best performance will be obtained using them. The total output capacitance value is usually determined by the desired output voltage ripple level and transient response requirements for sag (undershoot on positive load steps) and soar (overshoot on negative load steps).

### Output Ripple

Output ripple at the switching frequency is caused by the inductor current ripple and its effect on the output capacitor's ESR and stored charge. These two ripple components are called ESR ripple and capacitive ripple. Since ceramic capacitors have extremely low ESR and relatively little capacitance, both components are similar in amplitude and both should be considered if ripple is critical.

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} = \Delta I_L \times R_{ESR}$$

$$V_{RIPPLE(C)} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

For the Typical Operating Circuit for 1.05V output and an inductor ripple of 1A, with 2 x 22μF output capacitance each with about 10mΩ ESR including PCB trace resistance, the output voltage ripple components are :

$$V_{RIPPLE(ESR)} = 1A \times 5m\Omega = 5mV$$

$$V_{RIPPLE(C)} = \frac{1A}{8 \times 44\mu F \times 0.65MHz} = 4.4mV$$

$$V_{RIPPLE} = 5mV + 4.4mV = 9.4mV$$

### Output Transient Undershoot and Overshoot

In addition to voltage ripple at the switching frequency, the output capacitor and its ESR also affect the voltage sag (undershoot) and soar (overshoot) when the load steps up and down abruptly. The ACOT transient response is very quick and output transients are usually small. However, the combination of small ceramic output capacitors (with little capacitance), low output voltages (with little stored charge in the output capacitors), and low duty cycle applications (which require high inductance to get reasonable ripple currents with high input voltages) increases the size of voltage variations in response to very quick load changes. Typically, load changes occur slowly with respect to the IC's 650kHz switching frequency. But some modern digital loads can exhibit nearly instantaneous load changes and the following section shows how to calculate the worst-case voltage swings in response to very fast load steps.

The output voltage transient undershoot and overshoot each have two components : the voltage steps caused by the output capacitor's ESR, and the voltage sag and soar due to the finite output capacitance and the inductor current slew rate. Use the following formulas to check if the ESR is low enough (typically not a problem with ceramic capacitors) and the output capacitance is large enough to prevent excessive sag and soar on very fast load step edges, with the chosen inductor value.

The amplitude of the ESR step up or down is a function of the load step and the ESR of the output capacitor:

$$V_{ESR\_STEP} = \Delta I_{OUT} \times R_{ESR}$$

The amplitude of the capacitive sag is a function of the load step, the output capacitor value, the inductor value, the input-to-output voltage differential, and the maximum duty cycle. The maximum duty cycle during a fast transient is a function of the on-time and the minimum off-time since the ACOT™ control scheme will ramp the current using on-times spaced apart with minimum off-times, which is

as fast as allowed. Calculate the approximate on-time (neglecting parasitics) and maximum duty cycle for a given input and output voltage as :

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \text{ and } D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF(MIN)}}$$

The actual on-time will be slightly longer as the IC compensates for voltage drops in the circuit, but we can neglect both of these since the on-time increase compensates for the voltage losses. Calculate the output voltage sag as :

$$V_{SAG} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times (V_{IN(MIN)} \times D_{MAX} - V_{OUT})}$$

The amplitude of the capacitive soar is a function of the load step, the output capacitor value, the inductor value and the output voltage :

$$V_{SOAR} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times V_{OUT}}$$

For the Typical Operating Circuit for 1.05V output, the circuit has an inductor 1.4μH and 2 x 22μF output capacitance with 5mΩ ESR each. The ESR step is 3A x 2.5mΩ = 7.5mV which is small, as expected. The output voltage sag and soar in response to full 0A-3A-0A instantaneous transients are :

$$t_{ON} = \frac{1.05V}{12V \times 650kHz} = 135ns$$

$$\text{and } D_{MAX} = \frac{135ns}{135ns + 260ns} = 0.34$$

$$V_{SAG} = \frac{1.4\mu H \times (3A)^2}{2 \times 44\mu F \times (12V \times 0.34 - 1.05V)} = 47mV$$

$$V_{SOAR} = \frac{1.4\mu H \times (3A)^2}{2 \times 44\mu F \times 1.05V} = 136mV$$

The sag is about 4% of the output voltage and the soar is a full 13% of the output voltage. The ESR step is negligible here but it does partially add to the soar, so keep that in mind whenever using higher-ESR output capacitors.

The soar is typically much worse than the sag in high-input, low-output step-down converters because the high input voltage demands a large inductor value which stores lots of energy that is all transferred into the output if the load stops drawing current. Also, for a given inductor, the soar for a low output voltage is a greater voltage change and an even greater percentage of the output voltage. This is illustrated by comparing the previous to the next example.

The Typical Operating Circuit for 12V to 3.3V with a 2μH inductor and 2 x 22μF output capacitance can be used to illustrate the effect of a higher output voltage. The output voltage sag and soar in response to full 0A-3A-0A instantaneous transients are calculated as follows :

$$t_{ON} = \frac{3.3V}{12V \times 650kHz} = 423ns$$

$$\text{and } D_{MAX} = \frac{423ns}{423ns + 260ns} = 0.62$$

$$V_{SAG} = \frac{2\mu H \times (3A)^2}{2 \times 44\mu F \times (12V \times 0.62 - 3.3V)} = 49.5mV$$

$$V_{SOAR} = \frac{2\mu H \times (3A)^2}{2 \times 44\mu F \times 3.3V} = 62mV$$

In this case the sag is about 1.5% of the output voltage and the soar is only 2% of the output voltage.

Any sag is always short-lived, since the circuit quickly sources current to regain regulation in only a few switching cycles. With the RT2858B, any overshoot transient is typically also short-lived since the converter will sink current, reversing the inductor current sharply until the output reaches regulation again.

Most applications never experience instantaneous full load steps and the RT2858B's high switching frequency and fast transient response can easily control voltage regulation at all times. Also, since the sag and soar both are proportional to the square of the load change, if load steps were reduced to 1A (from the 3A examples preceding) the voltage changes would be reduced by a factor of almost ten. For these reasons sag and soar are seldom an issue except in very low-voltage CPU core or DDR memory supply applications, particularly for devices with high clock frequencies and quick changes into and out of sleep modes. In such applications, simply increasing the amount of ceramic output capacitor (sag and soar are directly proportional to capacitance) or adding extra bulk capacitance can easily eliminate any excessive voltage transients.

### Output Capacitors Stability Criteria

The RT2858B's ACOT™ control architecture uses an internal virtual inductor current ramp and other compensation that ensures stability with any reasonable output capacitor. The internal ramp allows the IC to operate with very low ESR capacitors and the IC is stable with very small capacitances. Therefore, output capacitor selection is nearly always a matter of meeting output voltage ripple and transient response requirements, as discussed in the previous sections. For the sake of the unusual application where ripple voltage is unimportant and there are few transients (perhaps battery charging or LED lighting) the stability criteria are discussed below.

The equations giving the minimum required capacitance for stable operation include a term that depends on the output capacitor's ESR. The higher the ESR, the lower the capacitance can be and still ensure stability. The equations can be greatly simplified if the ESR term is removed by setting ESR to zero. The resulting equation gives the worst-case minimum required capacitance and it is usually sufficiently small that there is usually no need for the more exact equation.

The required output capacitance ($C_{OUT}$) is a function of the inductor value (L) and the input voltage ($V_{IN}$) :

$$C_{OUT} \geq \frac{5.64 \times 10^{-11}}{V_{IN} \times L}$$

The worst-case high capacitance requirement is for low VIN and small inductance, so a 5V to 3.3V converter is used for an example. Using the inductance equation in a previous section to determine the required inductance :

$$L = \frac{3.3V \times (5V - 3.3V)}{5V \times 650kHz \times 1A} = 1.73\mu H$$

Therefore, the required minimum capacitance for the 5V to 3.3V converter is :

$$C_{OUT} \geq \frac{5.64 \times 10^{-11}}{5V \times 1.73\mu H} = 6.5\mu F$$

Using the 12V to 1.05V typical application as another example :

$$C_{OUT} \geq \frac{5.64 \times 10^{-11}}{12V \times 1.4\mu H} = 3.4\mu F$$

Any ESR in the output capacitor lowers the required minimum output capacitance, sometimes considerably. For the rare application where that is needed and useful, the equation including ESR is given here :

$$C_{OUT} \geq \frac{V_{OUT}}{2 \times f_{SW} \times V_{IN} \times (R_{ESR} + 13647 \times L \times V_{OUT})}$$

As can be seen, setting $R_{ESR}$ to zero and simplifying the equation yields the previous simpler equation. To allow for the capacitor's temperature and bias voltage coefficients, use at least double the calculated capacitance and use a good quality dielectric such as X5R or X7R with an adequate voltage rating since ceramic capacitors exhibit considerable capacitance reduction as their bias voltage increases.

## Applications Information

### Current-Sinking Applications

The RT2858B's is not recommended for current sinking applications even though its continuous switching operation allows the IC to sink some current. Sinking enables a fast recovery from output voltage overshoot caused by load transients and is normally useful for applications requiring negative currents, such as DDR $V_{TT}$ bus termination applications and changing-output voltage applications where the output voltage needs to slew quickly from one voltage to another. However, the IC's negative current limit is set low (about 1.6A) and the current limit behavior latches the synchronous rectifier off until the high-side switch's next pulse, to prevent the possibility of IC damage from large negative currents. Therefore, sinking current is not necessarily available at all times.

If implementing applications where current-sinking may occur, take care to allow for the current that is delivered to the input supply. A step-down converter in sinking operation functions like a backwards step-up converter. The current that is sunk at its output terminals is delivered up to its input terminals. If this current has no outlet, the input voltage will rise.

A good arrangement for long-term sinking applications is for a sinking supply (supply A) that is sinking current sourced from supply B, to both be powered by the same input supply. That way, any current delivered back to the input by supply A is current that just left the input through supply B. In this way, the current simply makes a round trip and the input supply will not rise.

In cases where this is not possible, make sure that there are sufficient other loads on the input supply to prevent that supply's voltage from rising high enough to cause damage to itself or any of its loads. In cases where the sinking is not long-term, such as output-voltage slewing applications, make sure there is sufficient input capacitance to control any input voltage rise. The worst-case voltage rise is :

$$\Delta V_{IN} = \frac{C_{OUT} \times \Delta V_{OUT}}{C_{IN}}$$

### Soft-Start (SS)

The RT2858B soft-start uses an external capacitor at SS to adjust the soft-start timing according to the following equation :

$$t_{SS}(ms) = \frac{C_{SS}\ (nF) \times 1.065V}{I_{SS}\ (\mu A)}$$

The available capacitance range is from 2.7nF to 220nF. If a 3.9nF capacitor is used, the typical soft-start will be 2ms. Do not leave SS unconnected.

### Enable Operation (EN)

For automatic start-up the high-voltage EN pin can be connected to $V_{IN}$, either directly or through a 100kΩ resistor. Its large hysteresis band makes EN useful for simple delay and timing circuits. EN can be externally pulled to $V_{IN}$ by adding a resistor-capacitor delay ($R_{EN}$ and $C_{EN}$ in Figure 1). Calculate the delay time using EN's internal threshold where switching operation begins (1.2V, typical).

An external MOSFET can be added to implement digital control of EN when no system voltage above 2V is available (Figure 2). In this case, a 100kΩ pull-up resistor, REN, is connected between VIN and the EN pin. MOSFET Q1 will be under logic control to pull down the EN pin. To prevent enabling circuit when VIN is smaller than the VOUT target value or some other desired voltage level, a resistive voltage divider can be placed between the input voltage and ground and connected to EN to create an additional input under-voltage lockout threshold (Figure 3).

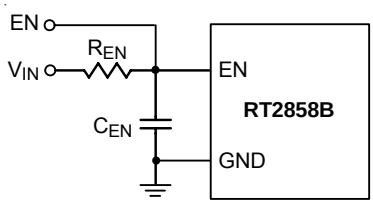



Figure 1. External Timing Control

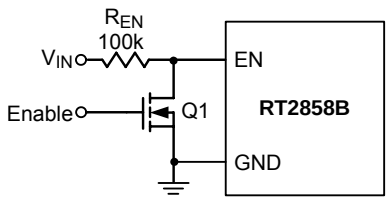



Figure 2. Digital Enable Control Circuit

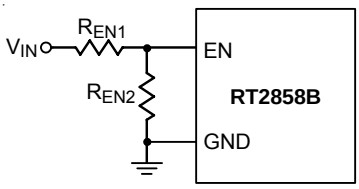



Figure 3. Resistor Divider for Lockout Threshold Setting

### Output Voltage Setting

Set the desired output voltage using a resistive divider from the output to ground with the midpoint connected to FB. The output voltage is set according to the following equation :

$$V_{OUT} = 0.765 \times (1 + \frac{R1}{R2})$$

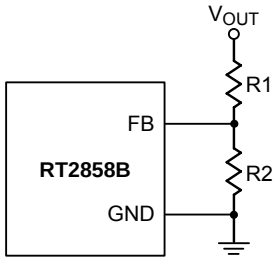



Figure 4. Output Voltage Setting

Place the FB resistors within 5mm of the FB pin. Choose R2 between 10kΩ and 100kΩ to minimize power consumption without excessive noise pick-up and calculate R1 as follows :

$$R1 = \frac{R2 \times (V_{OUT} - 0.765V)}{0.765V}$$

For output voltage accuracy, use divider resistors with 1% or better tolerance.

### Under-Voltage Lockout Protection

The RT2858B feature an Under-Voltage Lockout (UVLO) function that monitors the internal linear regulator output ($V_{PVDD}$) and prevents operation if $V_{PVDD}$ is too low. In some multiple input voltage applications, it may be desirable to use a power input that is too low to allow $V_{PVDD}$ to exceed the UVLO threshold. In this case, if there is another low-power supply available that is high enough to operate the $V_{PVDD}$ regulator, connecting that supply to VCC will allow the IC to operate, using the lower-voltage high-power supply for the DC/DC power path. Because of the internal linear regulator, any supply regulated or unregulated) between 4.5V and 18V will operate the IC.

### External BOOT Bootstrap Diode

When the input voltage is lower than 5.5V it is recommended to add an external bootstrap diode between VIN (or VCC) and the BOOT pin to improve enhancement of the internal MOSFET switch and improve efficiency. The bootstrap diode can be a low cost one such as 1N4148 or BAT54.

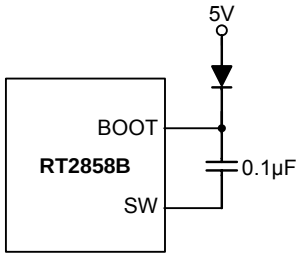



Figure 5. External Bootstrap Diode

### External BOOT Capacitor Series Resistance

The internal power MOSFET switch gate driver is optimized to turn the switch on fast enough for low power loss and good efficiency, but also slow enough to reduce EMI. Switch turn-on is when most EMI occurs since $V_{SW}$ rises rapidly. During switch turn-of, SW is discharged relatively slowly by the inductor current during the dead-time between high-side and low-switch on-times.

In some cases it is desirable to reduce EMI further, at the expense of some additional power dissipation. The switch turn-on can be slowed by placing a small (<10Ω) resistance between BOOT and the external bootstrap capacitor. This will slow the high-side switch turn-on and $V_{SW}$'s rise. To remove the resistor from the capacitor charging path (avoiding poor enhancement due to under-charging the BOOT capacitor), use the external diode shown in Figure 5 to charge the BOOT capacitor and place the resistance between BOOT and the capacitor/diode connection.

### $V_{PVDD}$ Capacitor Selection

Decouple $V_{PVDD}$ to PGND with a 1µF ceramic capacitor. High grade dielectric (X7R, or X5R) ceramic capacitors are recommended for their stable temperature and bias voltage characteristics.

### Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, $T_A$ is the ambient temperature, and $\theta_{JA}$ is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, $\theta_{JA}$, is layout dependent. For SOP-8 (Exposed Pad) package, the thermal resistance, $\theta_{JA}$, is 49°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at $T_A$ = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (49°C/W) = 2.041W for SOP-8 (Exposed Pad) package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, $\theta_{JA}$. The derating curve in Figure 6 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

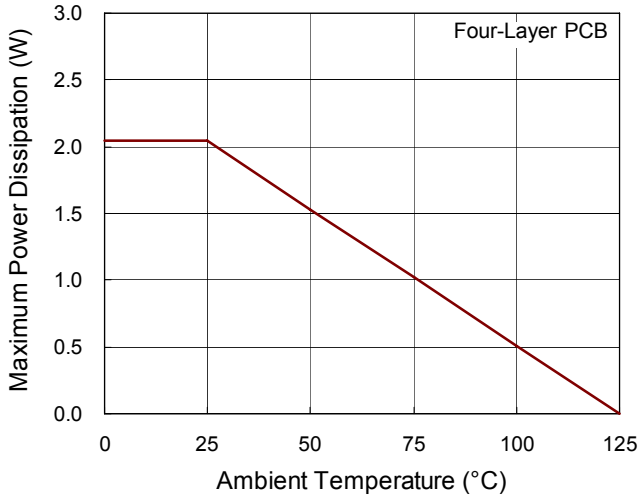
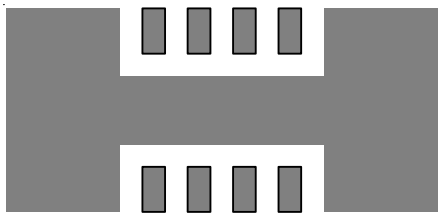



Figure 6. Derating Curve of Maximum Power Dissipation

### Recommendations for PCB Layout

- 1 Ounce Copper on Top Layer, plated-up through SMT PCB Mfg Process
- 1 Ounce Copper on Top Layer will improve Thermal performance Minimum 4 Layer PCB Stack up.
- Place the shape with 70mm$^2$ as Figure 7 around the PSOP-8 Footprint to achieve best thermal performance.



Copper Area = 70mm$^2$, $\theta_{JA}$ = 49°C/W

Figure 7. PCB Copper Area

- Utilize Standard PTH (Plated Through Hole, 25mil diameter, as Figure 8) to Via down from Exposed Pad on Top Layer, to GND Plane on PCB.

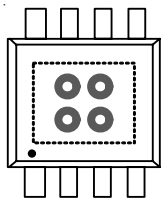


Figure 8. Standard PTH to GND Plane

### Layout Consideration

Follow the PCB layout guidelines for optimal performance of the RT2858B

- Keep the traces of the main current paths as short and wide as possible.
- Put the input capacitor as close as possible to the device pins (VIN and GND).
- SW node is with high frequency voltage swing and should be kept at small area. Keep sensitive components away from the SW node to prevent stray capacitive noise pickup.
- Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the RT2858B feedback pin.
- The GND and Exposed Pad should be connected to a strong ground plane for heat sinking and noise protection.

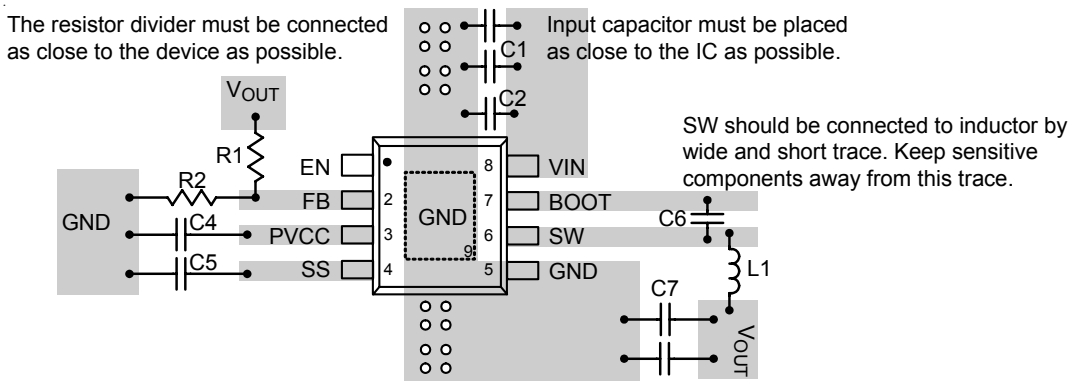
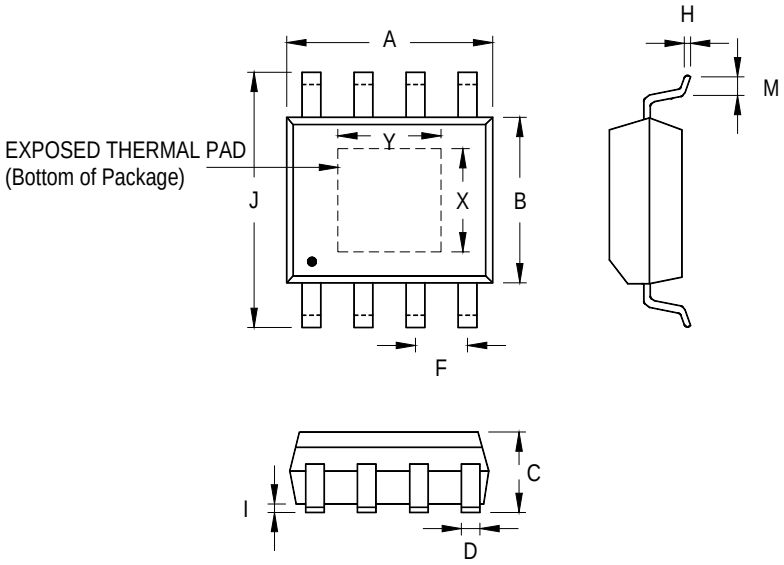



Figure 9. PCB Layout Guide

## Outline Dimension




| Symbol | | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|---|
| | | Min | Max | Min | Max |
| A | | 4.801 | 5.004 | 0.189 | 0.197 |
| B | | 3.810 | 4.000 | 0.150 | 0.157 |
| C | | 1.346 | 1.753 | 0.053 | 0.069 |
| D | | 0.330 | 0.510 | 0.013 | 0.020 |
| F | | 1.194 | 1.346 | 0.047 | 0.053 |
| H | | 0.170 | 0.254 | 0.007 | 0.010 |
| I | | 0.000 | 0.152 | 0.000 | 0.006 |
| J | | 5.791 | 6.200 | 0.228 | 0.244 |
| M | | 0.406 | 1.270 | 0.016 | 0.050 |
| Option 1 | X | 2.000 | 2.300 | 0.079 | 0.091 |
| | Y | 2.000 | 2.300 | 0.079 | 0.091 |
| Option 2 | X | 2.100 | 2.500 | 0.083 | 0.098 |
| | Y | 3.000 | 3.500 | 0.118 | 0.138 |

**8-Lead SOP (Exposed Pad) Plastic Package**

**Richtek Technology Corporation**

14F, No. 8, Tai Yuen 1st Street, Chupei City

Hsinchu, Taiwan, R.O.C.

Tel: (8863)5526789