

56F805

Evaluation Module User Manual

56F800
16-bit Digital Signal Controllers

DSP56F805EVMUM
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freescale.com



TABLE OF CONTENTS

Preface vii

Audience	vii
Organization	vii
Suggested Reading	vii
Notation Conventions	viii
Definitions, Acronyms, and Abbreviations	ix
References	x

Chapter 1 Introduction

1.1	56F805EVM Architecture	1-2
1.2	56F805EVM Configuration Jumpers	1-3
1.3	56F805EVM Connections	1-4

Chapter 2 Technical Summary

2.1	56F805	2-3
2.2	Program and Data Memory	2-4
2.3	RS-232 Serial Communications	2-5
2.4	Clock Source	2-6
2.5	Operating Mode	2-6
2.6	Debug LEDs	2-7
2.7	Debug Support	2-7
2.7.1	JTAG Connector	2-8
2.7.2	Parallel JTAG Interface Connector	2-9
2.8	External Interrupts	2-11
2.9	Reset	2-12
2.10	Power Supply	2-13
2.11	Primary UNI-3 Interface	2-14
2.12	Secondary UNI-3 Interface	2-15
2.13	General Purpose Switches and Run/Stop Switch	2-17
2.14	Serial 10-bit 4-channel D/A Converter	2-18
2.15	Motor Control PWM Signals and LEDs	2-19

2.16	Motor Protection Logic	2-19
2.16.1	Primary UNI-3 Motor Protection Logic	2-20
2.16.2	Secondary UNI-3 Motor Protection Logic	2-21
2.17	Back-EMF and Motor Phase Current Sensing	2-23
2.18	Quadrature Encoder/Hall-Effect Interface	2-24
2.19	Zero-Crossing Detection	2-24
2.20	CAN Interface	2-25
2.21	Software Feature Jumpers	2-26
2.22	Peripheral Connectors	2-27
2.22.1	Port B Expansion Connector	2-27
2.22.2	Port D Expansion Connector	2-28
2.22.3	Port E Expansion Connector	2-28
2.22.4	External Memory Control Signal Expansion Connector	2-29
2.22.5	Primary Encoder/Timer Channel A Expansion Connector	2-29
2.22.6	Secondary Encoder/Timer Channel B Expansion Connector	2-30
2.22.7	Timer Channel C Expansion Connector	2-30
2.22.8	Timer Channel D Expansion Connector	2-31
2.22.9	Address Bus Expansion Connector	2-32
2.22.10	Data Bus Expansion Connector	2-33
2.22.11	A/D Port Expansion Connector	2-33
2.22.12	Serial Communications Port 0 Expansion Connector	2-34
2.22.13	Serial Communications Port 1 Expansion Connector	2-34
2.22.14	Serial Peripheral Interface Expansion Connector	2-35
2.22.15	CAN Expansion Connector	2-35
2.22.16	PWM Port A Expansion Connector	2-36
2.22.17	PWM Port B Expansion Connector	2-37
2.23	Secondary UNI-3 Unattached Signal Connector	2-38
2.24	Test Points	2-38

Appendix A
56F805EVM Schematics

Appendix B
56F805EVM Bill of Material


LIST OF FIGURES

1-1	Block Diagram of the 56F805EVM	1-2
1-2	56F805EVM Jumper Reference	1-3
1-3	Connecting the 56F805EVM Cables	1-4
2-1	Schematic Diagram of the External Memory Interface	2-4
2-2	Schematic Diagram of the RS-232 Interface	2-5
2-3	Schematic Diagram of the Clock Interface	2-6
2-4	Schematic Diagram of the Debug LED Interface	2-7
2-5	Block Diagram of the Parallel JTAG Interface	2-9
2-6	Schematic Diagram of the User Interrupt Interface	2-11
2-7	Schematic Diagram of the RESET Interface	2-12
2-8	Schematic Diagram of the Power Supply	2-13
2-9	Run/Stop and General Purpose Switches	2-17
2-10	Serial 10-bit, 4-Channel D/A Converter	2-18
2-11	PWM Group A Interface and LEDs	2-19
2-12	FAULTA1 Selection Circuit	2-20
2-13	DC-Bus Over-Voltage and Phase Over-Current Detection Circuits	2-21
2-14	FAULTB1 Selection Circuit	2-22
2-15	Primary Back-EMF or Motor Phase Current Sense Signals	2-23
2-16	Zero-Crossing Encoder Interface	2-24
2-17	CAN Interface	2-25
2-18	Software Feature Jumpers	2-26
A-1	56F801 Processor	A-2
A-2	Reset, Mode, Clock & IRQs	A-3
A-3	Program & Data SRAM Memory	A-4
A-4	RS-232 and SCI Connectors	A-5
A-5	Debug Serial D/A Converter	A-6
A-6	PWM A AND Three User LEDs	A-7
A-7	Primary UNI-3 Interface	A-8

A-8	Secondary UNI-3 Back-EMF, Over-Voltage and Over-Current Sense	A-9
A-9	User General Purpose Switches and Jumpers	A-10
A-10	Motor Phase-Current/Back-EMF Voltage Analog Input Selector	A-11
A-11	Primary and Secondary 3-Phase Over-Current Sense	A-12
A-12	Primary Zero-Crossing/Quadrature-Encoder or Hall-Effect Selector	A-13
A-13	Secondary Zero-Crossing/Quadrature-Encoder or Hall-Effect Selector	A-14
A-14	Port Expansion Connectors	A-15
A-15	High-Speed CAN Interface	A-16
A-16	Parallel JTAG Host Target Interface and JTAG Connector	A-17
A-17	Power Supplies	A-18
A-18	Bypass Capacitors and Spare Gates	A-19

LIST OF TABLES

1-1	56F805EVM Default Jumper Options	1-3
2-1	RS-232 Serial Connector Description	2-5
2-2	Operating Mode Selection	2-6
2-3	JTAG Connector Description.	2-8
2-4	Parallel JTAG Interface Disable Jumper Selection	2-8
2-5	Parallel JTAG Interface Connector Description	2-9
2-6	On-Board Host Target Interface Power Source Jumper Selection	2-10
2-7	Primary UNI-3 Connector Description	2-14
2-8	Secondary UNI-3 Connector Description	2-15
2-9	Unused Secondary UNI-3 Connector Signal Description	2-16
2-10	D/A Header Description.	2-18
2-11	FAULTA1 Source Selection Jumper	2-20
2-12	FAULTB1 Source Selection Jumper	2-22
2-13	CAN Header Description.	2-26
2-14	Port B Connector Description	2-27
2-15	Port D Connector Description	2-28
2-16	Port E Connector Description	2-28
2-17	External Memory Control Signal Connector Description	2-29
2-18	Timer A Connector Description.	2-29
2-19	Timer B Connector Description	2-30
2-20	Timer C Connector Description	2-30
2-21	Timer D Connector Description.	2-31
2-22	External Memory Address Bus Connector Description.	2-32
2-23	External Memory Address Bus Connector Description.	2-33
2-24	A/D Connector Description	2-33
2-25	SCI0 Connector Description	2-34
2-26	SCI1 Connector Description	2-34



2-27	SPI Connector Description	2-35
2-28	CAN Connector Description	2-35
2-29	PWM Port A Connector Description	2-36
2-30	PWM Port B Connector Description	2-37
2-31	Secondary UNI-3 Unattached Signal Connector Description	2-38

Preface

This reference manual describes in detail the hardware on the 56F805 Evaluation Module.

Audience

This document is intended for application developers who are creating software for devices using the Freescale 56F805 part.

Organization

This manual is organized into two chapters and two appendixes.

- **Chapter 1, Introduction** - provides an overview of the EVM and its features.
- **Chapter 2, Technical Summary** - describes in detail the 56F805EVM hardware.
- **Appendix A, 56F805EVM Schematics** - contains the schematics of the 56F805EVM.
- **Appendix B, 56F805EVM Bill of Material** - provides a list of the materials used on the 56F805EVM board.

Suggested Reading

Documentation on the 56F805 and the 56F805EVM kit may be found at this URL:

<http://www.freescale.com>

Notation Conventions

This document uses the following conventions:

Term or Value	Symbol	Examples	Exceptions
Active High Signals (Logic One)	No special symbol attached to the signal name	A0 CLKO	
Active Low Signals (Logic Zero)	Noted with an overbar in text and in most figures	\overline{WE} \overline{OE}	In schematic drawings, Active Low Signals may be noted by a backslash: /WE
Hexadecimal Values	Begin with a "\$" symbol	\$0FF0 \$80	
Decimal Values	No special symbol attached to the number	10 34	
Binary Values	Begin with the letter "b" attached to the number	b1010 b0011	
Numbers	Considered positive unless specifically noted as a negative value	5 -10	Voltage is often shown as positive: +3.3V
Bold	Reference sources, paths, emphasis	...see: http://www.freescale.com	

Definitions, Acronyms, and Abbreviations

Definitions, acronyms and abbreviations for terms used in this document are defined below for reference.

A/D	Analog-to-Digital
CAN	Controller Area Network, a serial communications peripheral and method
CiA	CAN in Automation, an international CAN user's group that coordinates standards for CAN communications protocols
D/A	Digital-to-Analog
EVM	Evaluation Module
GPIO	General Purpose Input and Output Port
IC	Integrated Circuit
JTAG	Joint Test Action Group, a bus protocol/interface used for test and debug
LQFP	Low-profile Quad Flat Pack
MPIO	Multi Purpose Input and Output Port; shares package pins with other peripherals on the chip and can function as a GPIO
OnCE™	On-Chip Emulation, a debug bus and port created by Freescale to enable designers to create a low-cost hardware interface for a professional-quality debug environment
PCB	Printed Circuit Board
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
RAM	Random Access Memory
ROM	Read-Only Memory
SCI	Serial Communications Interface
SPI	Serial Peripheral Interface Port
SRAM	Static Random Access Memory
UART	Universal Asynchronous Receiver/Transmitter

References

The following sources were referenced to produce this manual:

- [1] *DSP56800 Family Manual*, Freescale Semiconductor, DSP56800FM
- [2] *DSP56F801/803/805/807 User's Manual*, Freescale Semiconductor, DSP56F801-7UM
- [3] *56F805 Technical Data*, Freescale Semiconductor, DSP56F805
- [4] *CiA Draft Recommendation DR-303-1, Cabling and Connector Pin Assignment*, Version 1.0, CAN in Automation
- [5] *CAN Specification 2.0B*, BOSCH or CAN in Automation

Chapter 1

Introduction

The 56F805EVM is used to demonstrate the abilities of the 56F805 and to provide a hardware tool allowing the development of applications that use the 56F805.

The 56F805EVM is an evaluation module board that includes a 56F805 part, peripheral expansion connectors, external memory and a CAN interface. The expansion connectors are for signal monitoring and user feature expandability.

The 56F805EVM is designed for the following purposes:

- Allowing new users to become familiar with the features of the 56800 architecture. The tools and examples provided with the 56F805EVM facilitate evaluation of the feature set and the benefits of the family.
- Serving as a platform for real-time software development. The tool suite enables the user to develop and simulate routines, download the software to on-chip or on-board RAM, run it, and debug it using a debugger via the JTAG/OnCE™ port. The breakpoint features of the OnCE port enable the user to easily specify complex break conditions and to execute user-developed software at full-speed, until the break conditions are satisfied. The ability to examine and modify all user accessible registers, memory and peripherals through the OnCE port greatly facilitates the task of the developer.
- Serving as a platform for hardware development. The hardware platform enables the user to connect external hardware peripherals. The on-board peripherals can be disabled, providing the user with the ability to reassign any and all of the controller's peripherals. The OnCE port's unobtrusive design means that all of the memory on the board and on the chip are available to the user.

1.1 56F805EVM Architecture

The 56F805EVM facilitates the evaluation of various features present in the 56F805 part. The 56F805EVM can be used to develop real-time software and hardware products based on the 56F805. The 56F805EVM provides the features necessary for a user to write and debug software, demonstrate the functionality of that software and interface with the customer's application-specific device(s). The 56F805EVM is flexible enough to allow a user to fully exploit the 56F805's features to optimize the performance of his product, as shown in [Figure 1-1](#).

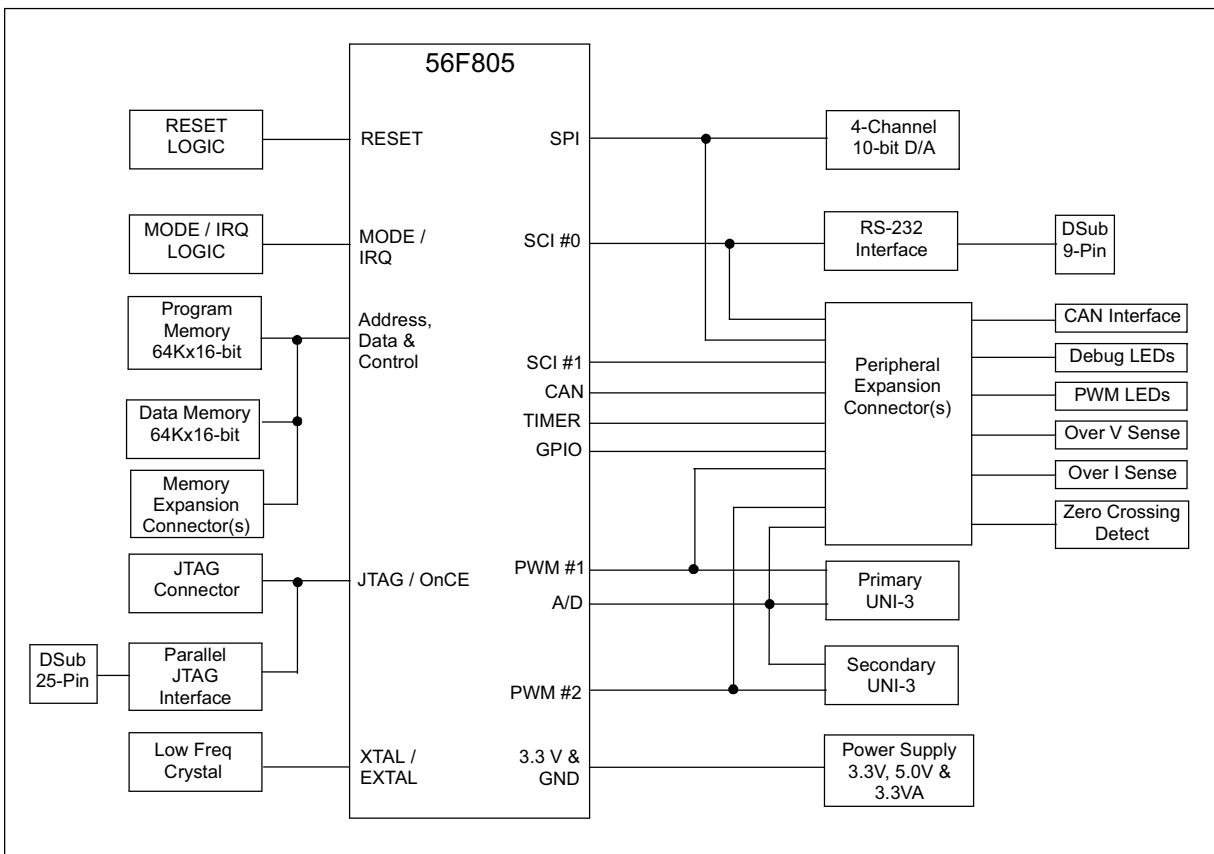


Figure 1-1. Block Diagram of the 56F805EVM

Table 1-1. 56F805EVM Default Jumper Options (Continued)

Jumper Group	Comment	Jumpers Connections
JG10	Secondary UNI-3 Analog Temperature Input unused	1-2
JG11	Use Host power for Host Target Interface	1-2
JG12	Primary Encoder Input Selected	2-3, 5-6 & 8-9
JG13	Secondary Encoder Input Selected	2-3, 5-6 & 8-9
JG14	Primary UNI-3 3-Phase Current Sense Selected as Analog Inputs	2-3, 5-6 & 8-9
JG15	Primary UNI-3 Phase A Over-Current Selected for FAULTA1	1-2
JG16	Secondary UNI-3 Phase B Over-Current Selected for FAULTB1	1-2
JG17	CAN termination unselected	NC
JG18	Use on-board crystal for oscillator input	1-2

1.3 56F805EVM Connections

An interconnection diagram is shown in [Figure 1-3](#) for connecting the PC and the external +12V DC power supply to the 56F805EVM board.

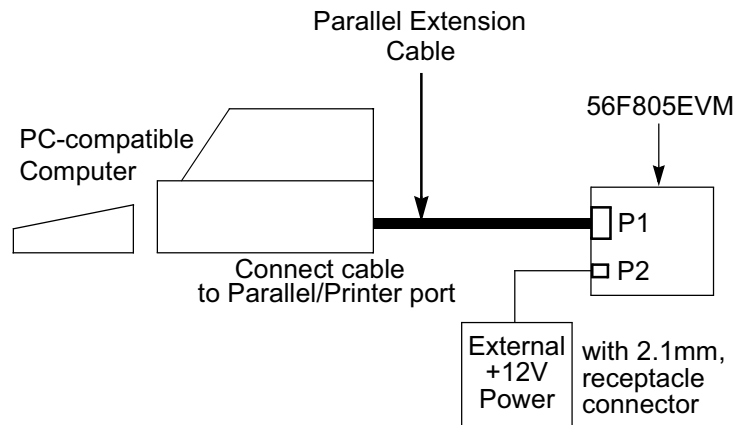


Figure 1-3. Connecting the 56F805EVM Cables

Perform the following steps to connect the 56F805EVM cables:

1. Connect the parallel extension cable to the Parallel port of the host computer
2. Connect the other end of the parallel extension cable to P1, shown in **Figure 1-3**, on the 56F805EVM board. This provides the connection which allows the host computer to control the board.
3. Make sure that the external +12V DC, 4.0A power supply is not plugged into a 120V AC power source
4. Connect the 2.1mm output power plug from the external power supply into P2, shown in **Figure 1-3**, on the 56F805EVM board
5. Apply power to the external power supply. The green Power-On LED, LED10, will illuminate when power is correctly applied.



Chapter 2

Technical Summary

The 56F805EVM is designed as a versatile controller development card for developing real-time software and hardware products to support a new generation of applications in digital and wireless messaging, servo and motor control, digital answering machines, feature phones, modems, and digital cameras. The power of the 16-bit 56F805 controller, combined with the on-board 64K × 16-bit external program static RAM (SRAM), 64K × 16-bit external data SRAM, CAN interface, Hall-Effect/Quadrature Encoder interface, motor zero crossing logic, motor bus over-current logic, motor bus over-voltage logic and parallel JTAG interface, makes the 56F805EVM ideal for developing and implementing many motor controlling algorithms, as well as for learning the architecture and instruction set of the 56F805 processor.

The main features of the 56F805EVM include:

- 56F805 16-bit +3.3V controller operating at 80MHz [U1]
- External fast static RAM (FSRAM) memory [U15], configured as:
 - 64K×16 bits of program memory with 0 wait states at 70MHz
 - 64K×16 bits of data memory with 0 wait states at 70MHz
- 4-Channel 10-bit Serial D/A, SPI for real-time user data display [U18]
- 8.00MHz crystal oscillator for frequency generation [Y1]
- Optional external oscillator frequency input connector [JG6 and JG18]
- Joint Test Action Group (JTAG) port interface connector for an external debug Host Target Interface [J29]
- On-board Parallel JTAG Host Target Interface, with a connector for a PC printer port cable [P1]
- RS-232 interface for easy connection to a host processor [U16 and P3]
- CAN interface for high speed, 1.0Mbps, communications [U20 and J26]
- CAN bypass and bus termination [J32 and JG17]
- Connector to allow the user to connect his own SPI0 / MPIO-compatible peripheral [J16]

- Connector to allow the user to connect his own SCI1 / MPIO-compatible peripheral [J17]
- Connector to allow the user to connect his own SPI / MPIO-compatible peripheral [J19]
- Connector to allow the user to connect his own PWMA or MPIO-compatible peripheral [J21]
- Connector to allow the user to connect his own PWMB / MPIO-compatible peripheral [J22]
- Connector to allow the user to connect his own CAN physical layer peripheral [J25]
- Connector to allow the user to connect his own Timer A / MPIO-compatible peripheral [J3]
- Connector to allow the user to connect his own Timer B / MPIO-compatible peripheral [J6]
- Connector to allow the user to connect his own Timer C / MPIO-compatible peripheral [J8]
- Connector to allow the user to connect his own Timer D / MPIO-compatible peripheral [J5]
- Connector to allow the user to attach his own Port B GPIO-compatible peripheral [J28]
- Connector to allow the user to attach his own Port D GPIO-compatible peripheral [J4]
- Connector to allow the user to attach his own Port E GPIO-compatible peripheral [J7]
- 56F805's external memory expansion connectors [J1, J2 and J27]
- On-board power regulation from an external +12V DC-supplied power input [P2]
- Light Emitting Diode (LED) power indicator [LED10]
- Three on-board real-time user debugging LEDs [LED1-3]
- Six on-board Primary PWM monitoring LEDs [LED4-9]
- Primary UNI-3 Motor interface [J30]
 - Encoder/Hall-Effect interface
 - Over-Voltage sensing [U8]
 - Over-Current sensing [U5]
 - Phase Current sensing [U8 and U21]
 - Back-EMF sensing
 - Temperature sensing
 - Zero Crossing detection
 - Pulse Width Modulation

- Secondary UNI-3 Motor interface [J31]
 - Encoder/Hall-Effect interface
 - Over-Voltage sensing [U6]
 - Over-Current sensing [U22]
 - Phase Current sensing [U6 and U7]
 - Back-EMF sensing
 - Temperature sensing
 - Zero Crossing detection
 - Pulse Width Modulation
- Manual RESET push-button [S1]
- Manual interrupt push-button for $\overline{\text{IRQA}}$ [S2]
- Manual interrupt push-button for $\overline{\text{IRQB}}$ [S3]
- General purpose push-button on GPIO PD3 [S4]
- General purpose push-button on GPIO PD4 [S5]
- General purpose toggle switch for RUN/STOP control(PD5) [S6]

2.1 56F805

The 56F805EVM uses a Freescale DSP56F805FV80 part, designated as U1 on the board and in the schematics. This part will operate at a maximum speed of 80MHz. A full description of the 56F805, including functionality and user information, is provided in the following documents:

- *DSP56800 Family Manual*, (DSP56800FM): Provides a detailed description of the core processor, including internal status and control registers and a detailed description of the family instruction set.
- *DSP56F801/803/805/807 User's Manual*, (DSP56F801-7UM): Provides an overview description of the controller and detailed information about the on-chip components including the memory and I/O maps, peripheral functionality, and control/status register descriptions for each subsystem.
- *56F805 Technical Data*, (DSP56F805): Provides features list and specifications including signal descriptions, DC power requirements, AC timing requirements and available packaging.

Refer to these documents for detailed information about chip functionality and operation. They can be found on the following URL:

<http://www.freescale.com>

2.2 Program and Data Memory

The 56F805EVM uses one bank of 128K×16-bit Fast Static RAM (GSI GS72116, labeled U15) for external memory expansion; see the FSRAM schematic diagram in [Figure 2-1](#). This physical memory bank is split into two logical memory banks of 64K×16-bits: one for Program memory and the other for Data memory. By using the device's program strobe, \overline{PS} , signal line, along with the memory chip's A0 signal line, half of the memory chip is selected when Program memory accesses are requested and the other half of the memory chip is selected when Data memory accesses are requested. This memory bank will operate with zero wait-state accesses while the 56F805 is running at 70MHz. However, when running at 80MHz, the memory bank operates with four wait-state accesses. This memory bank can be disabled by removing the jumper at JG8.

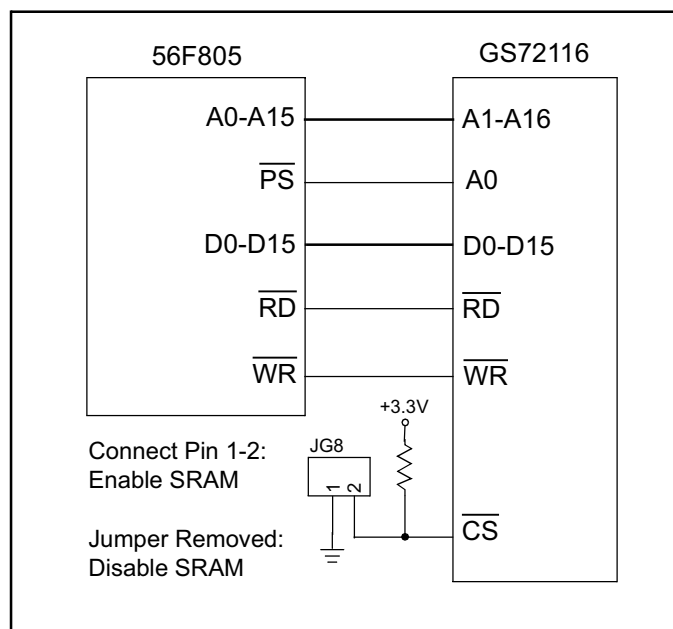


Figure 2-1. Schematic Diagram of the External Memory Interface

2.3 RS-232 Serial Communications

The 56F805EVM provides an RS-232 interface by the use of an RS-232 level converter, (Analog Devices ADM3311EARS, designated as U16); refer to the RS-232 schematic diagram in [Figure 2-2](#). The RS-232 level converter transitions the SCI UART's +3.3V signal levels to RS-232 compatible signal levels and connects to the host's serial port via connector P3. Flow control is not provided, but could be implemented using uncommitted GPIO signals. The pinout of connector P3 is listed in [Table 2-1](#). The RS-232 level converter/transceiver can be disabled by removing the jumper at JG9.

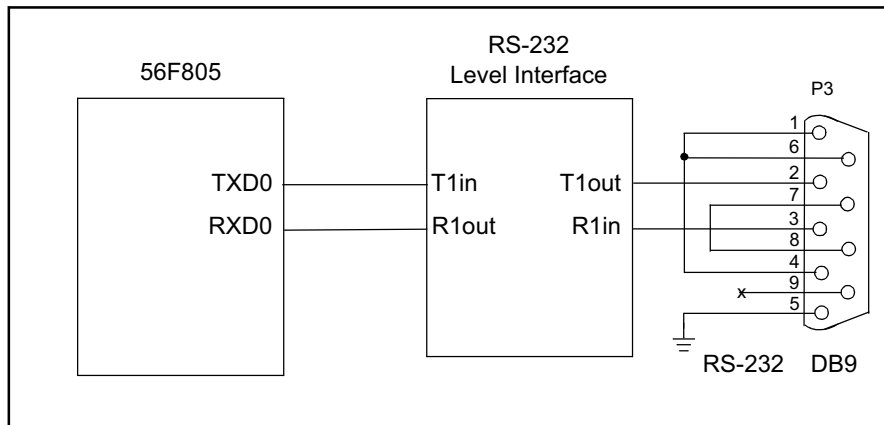


Figure 2-2. Schematic Diagram of the RS-232 Interface

Table 2-1. RS-232 Serial Connector Description

P3			
Pin #	Signal	Pin #	Signal
1	Jumper to 6 & 4	6	Jumper to 1 & 4
2	TXD	7	Jumper to 8
3	RXD	8	Jumper to 7
4	Jumper to 1 & 6	9	N/C
5	GND		

2.4 Clock Source

The 56F805EVM uses an 8.00MHz crystal, Y1, connected to its External Crystal Inputs, EXTAL and XTAL. The 56F805 uses its internal PLL to multiply the input frequency by 10 to achieve its 80MHz maximum operating frequency. An external oscillator source can be connected to the controller by using the oscillator bypass connectors, JG6 and JG18; see [Figure 2-3](#).

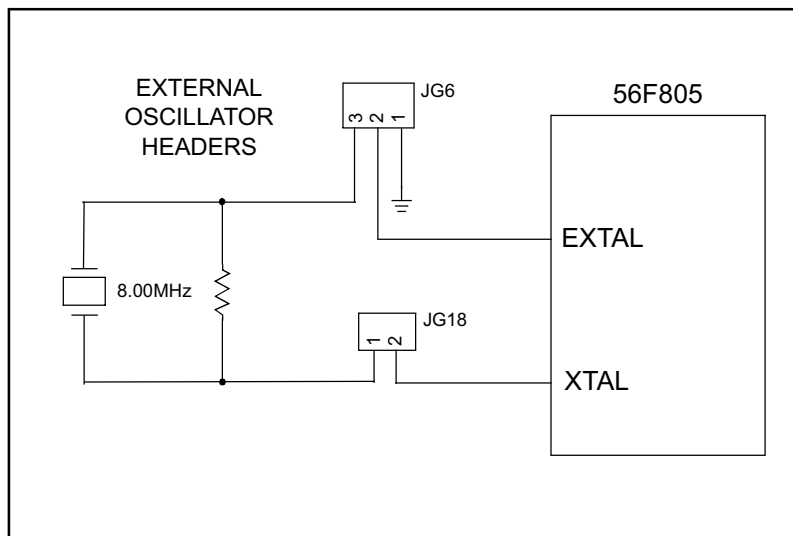


Figure 2-3. Schematic Diagram of the Clock Interface

2.5 Operating Mode

The 56F805EVM provides a boot-up MODE selection jumper, JG7. This jumper is used to select the operating mode of the device as it exits RESET. Refer to the DSP56F801/803/805/807 User's Manual for a complete description of the chip's operating modes. [Table 2-2](#) shows the two operation modes available on the 56F805.

Table 2-2. Operating Mode Selection

Operating Mode	JG7	Comment
0	1–2	Bootstrap from internal memory (GND)
3	No Jumper	Bootstrap from external memory (+3.3V)

2.6 Debug LEDs

Three on-board Light-Emitting Diodes, (LEDs), are provided to allow real-time debugging for user programs. These LEDs will allow the programmer to monitor program execution without having to stop the program during debugging; refer to [Figure 2-4](#). User LED1 is controlled by Port B's PB0 signal. User LED2 is controlled by PB1. User LED3 is controlled by PB2. Setting PB0, PB1 or PB2 to a Logic One value will turn on the associated LED.

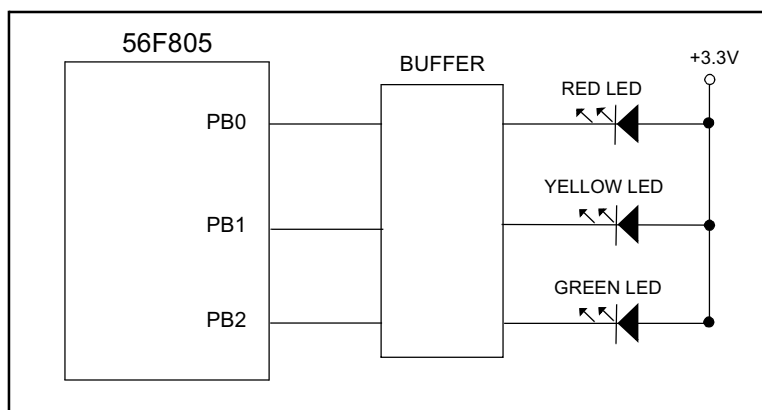


Figure 2-4. Schematic Diagram of the Debug LED Interface

2.7 Debug Support

The 56F805EVM provides an on-board Parallel JTAG Host Target Interface and a JTAG interface connector for external Target Interface support. Two interface connectors are provided to support each of these debugging approaches. These two connectors are designated the JTAG connector and the Host Parallel Interface Connector.

2.7.1 JTAG Connector

The JTAG connector on the 56F805EVM allows the connection of an external Host Target Interface for downloading programs and working with the 56F805's registers. This connector is used to communicate with an external Host Target Interface which passes information and data back and forth with a host processor running a debugger program. [Table 2-3](#) shows the pin-out for this connector.

Table 2-3. JTAG Connector Description

J29			
Pin #	Signal	Pin #	Signal
1	TDI	2	GND
3	TDO	4	GND
5	TCK	6	GND
7	NC	8	KEY
9	$\overline{\text{RESET}}$	10	TMS
11	+3.3V	12	NC
13	NC	14	$\overline{\text{TRST}}$

When this connector is used with an external Host Target Interface, the parallel JTAG interface should be disabled by placing a jumper in jumper block JG5. Reference [Table 2-4](#) for this jumpers selection options.

Table 2-4. Parallel JTAG Interface Disable Jumper Selection

JG5	Comment
No jumpers	On-board Parallel JTAG Interface Enabled
1–2	Disable on-board Parallel JTAG Interface

2.7.2 Parallel JTAG Interface Connector

The Parallel JTAG Interface Connector, P1, allows the 56F805 to communicate with a Parallel Printer Port on a Windows PC; refer to [Figure 2-5](#). By using this connector, the user can download programs and work with the 56F805's registers. [Table 2-5](#) shows the pin-out for this connector. When using the parallel JTAG interface, the jumper at JG5 should be removed, as shown in [Table 2-4](#). A jumper, JG11, is provided to allow the on-board Host/Target Interface to be powered by the Target board instead of the Host system when necessary; reference [Table 2-6](#). This may be necessary when using a +3.3V Host computer parallel port.

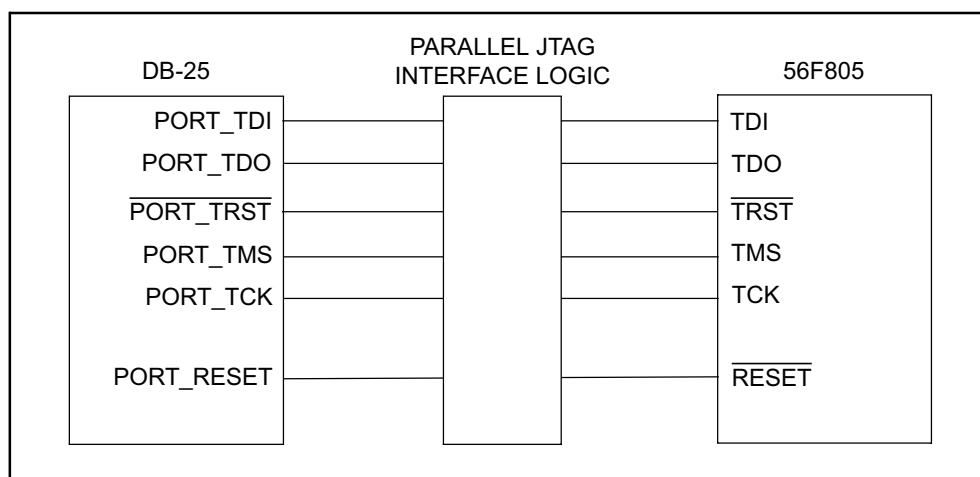


Figure 2-5. Block Diagram of the Parallel JTAG Interface

Table 2-5. Parallel JTAG Interface Connector Description

P1			
Pin #	Signal	Pin #	Signal
1	NC	14	NC
2	PORT_RESET	15	PORT_IDENT
3	PORT_TMS	16	NC
4	PORT_TCK	17	NC
5	PORT_TDI	18	GND
6	$\overline{\text{PORT_TRST}}$	19	GND
7	NC	20	GND

Table 2-5. Parallel JTAG Interface Connector Description (Continued)

P1			
Pin #	Signal	Pin #	Signal
8	PORT_IDENT	21	GND
9	PORT_VCC	22	GND
10	NC	23	GND
11	PORT_TDO	24	GND
12	NC	25	GND
13	PORT_CONNECT		

Table 2-6. On-Board Host Target Interface Power Source Jumper Selection

JG11	Comment
1-2	Host supplied power
2-3	Target supplied power

2.8 External Interrupts

Two on-board push-button switches are provided for external interrupt generation, as shown in [Figure 2-6](#). S1 allows the user to generate a hardware interrupt for signal line $\overline{\text{IRQA}}$. S2 allows the user to generate a hardware interrupt for signal line $\overline{\text{IRQB}}$. These two switches allow the user to generate interrupts for his user-specific programs.

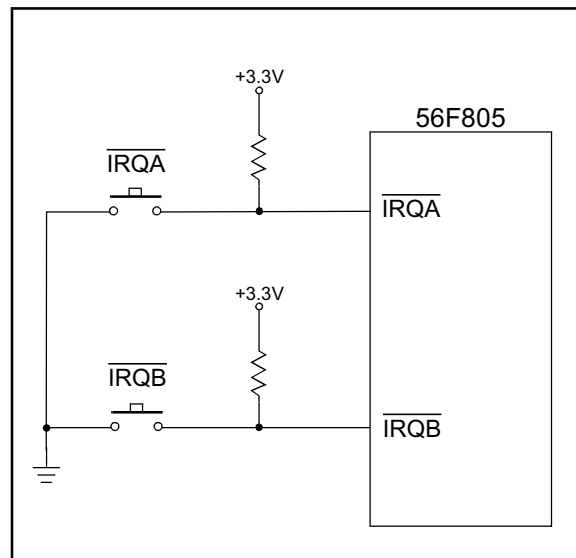


Figure 2-6. Schematic Diagram of the User Interrupt Interface

2.9 Reset

Logic is provided on the 56F805 to generate a clean power-on RESET signal. Additional, reset logic is provided to support the RESET signals from the JTAG connector, the Parallel JTAG Interface and the user RESET push-button; see [Figure 2-7](#).

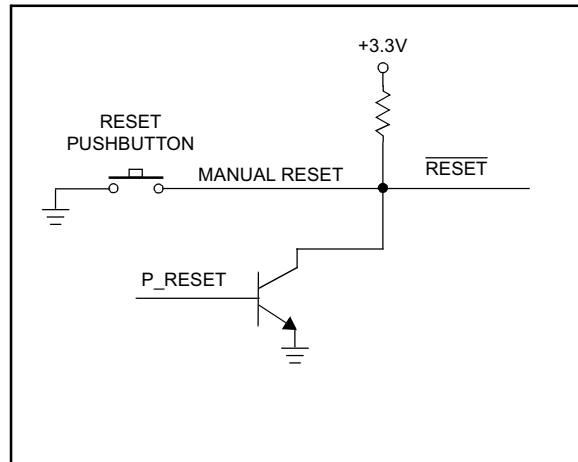


Figure 2-7. Schematic Diagram of the RESET Interface

2.10 Power Supply

The main power input, 12V DC at 4.0A, to the 56F805EVM is through a 2.1mm coax power jack. A 4.0Amp power supply is provided with the 56F805EVM; however, less than 500mA is required by the EVM. The remaining current is available for user motor control applications when connected to an optional motor power stage board. The 56F805EVM provides +3.3V DC voltage regulation for the device, memory, D/A, CAN, parallel JTAG interface and supporting logic; refer to [Figure 2-8](#). Power applied to the 56F805EVM is indicated with a Power-On LED, referenced as LED10.

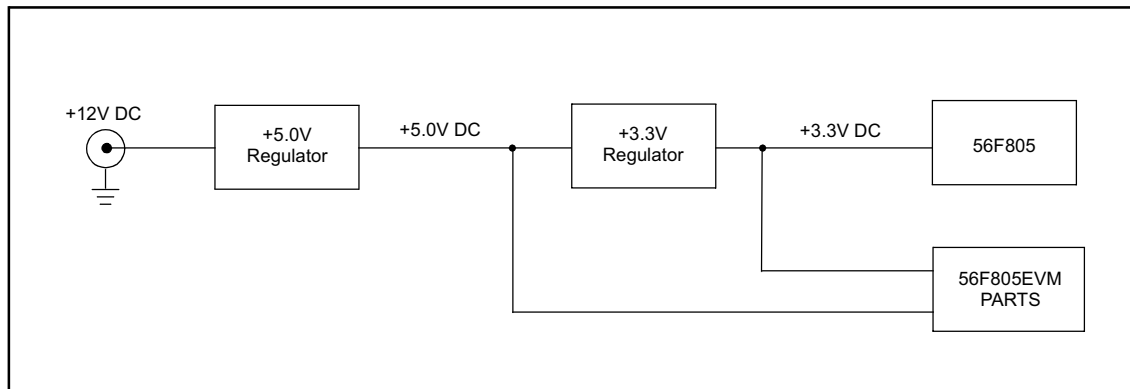


Figure 2-8. Schematic Diagram of the Power Supply

2.11 Primary UNI-3 Interface

Motor control signals from a family of motor driver boards can be connected to the EVM board via the Primary UNI-3 connector/interface. The Primary UNI-3 connector/interface contains all of the signals needed to drive and control the motor drive boards. These signals are connected to differing groups of the controller's input and output ports: A/D, TIMER and PWM A. Refer to [Table 2-7](#) for the pin out of the Primary UNI-3 connector.

Table 2-7. Primary UNI-3 Connector Description

J30			
Pin #	Signal	Pin #	Signal
1	PWM_AT	2	Shield
3	PWM_AB	4	Shield
5	PWM_BT	6	Shield
7	PWM_BB	8	Shield
9	PWM_CT	10	Shield
11	PWM_CB	12	GND
13	GND	14	+5.0V DC
15	+5.0V DC	16	Analog +3.3V DC
17	Analog GND	18	Analog GND
19	Analog +15V DC	20	Analog -15V DC
21	Motor DC Bus Voltage Sense	22	Motor DC Bus Current Sense
23	Motor Phase A Current Sense	24	Motor Phase B Current Sense
25	Motor Phase C Current Sense	26	Motor Drive Temperature Sense
27	NC	28	Shield
29	Motor Drive Brake Control	30	Serial COM
31	PFC PWM	32	PFC Inhibit
33	PFC Zero Cross	34	Zero Cross A

Table 2-7. Primary UNI-3 Connector Description (Continued)

J30			
Pin #	Signal	Pin #	Signal
35	Zero Cross B	36	Zero Cross C
37	Shield	38	Back-EMF Phase A Sense
39	Back-EMF Phase B Sense	40	Back-EMF Phase C Sense

2.12 Secondary UNI-3 Interface

A Secondary UNI-3 Motor Drive interface is available on the EVM board. Motor control signals from a family of motor driver boards can be connected to the EVM board via the Secondary UNI-3 connector/interface. The Secondary UNI-3 connector/interface contains a majority of the signals needed to drive and control the motor drive boards. The unused signals are connected to a header, J14. These signals are connected to differing groups of the controller's input and output ports: A/D, TIMER and PWM B. Refer to [Table 2-8](#) for the pin out of the Secondary UNI-3 connector and to [Table 2-9](#) for the pin out of the unused signal header.

Table 2-8. Secondary UNI-3 Connector Description

J31			
Pin #	Signal	Pin #	Signal
1	PWM_AT	2	Shield
3	PWM_AB	4	Shield
5	PWM_BT	6	Shield
7	PWM_BB	8	Shield
9	PWM_CT	10	Shield
11	PWM_CB	12	GND
13	GND	14	NC
15	NC	16	NC
17	Analog GND	18	Analog GND
19	NC	20	NC

Table 2-8. Secondary UNI-3 Connector Description (Continued)

J31			
Pin #	Signal	Pin #	Signal
21	Motor DC Bus Voltage Sense	22	Motor DC Bus Current Sense
23	Motor Phase A Current Sense	24	Motor Phase B Current Sense
25	Motor Phase C Current Sense	26	Motor Drive Temperature Sense
27	NC	28	Shield
29	Motor Drive Brake Control	30	Serial COM
31	PFC PWM	32	PFC Inhibit
33	PFC Zero Cross	34	Zero Cross A
35	Zero Cross B	36	Zero Cross C
37	Shield	38	Back-EMF Phase A Sense
39	Back-EMF Phase B Sense	40	Back-EMF Phase C Sense

Table 2-9. Unused Secondary UNI-3 Connector Signal Description

J14			
Pin #	Signal	Pin #	Signal
1	SU3_ZERO_X_A	2	SU3_ZERO_X_B
3	SU3_ZERO_X_C	4	SU3_BK_EMF_A
5	SU3_BK_EMF_B	6	SU3_BK_EMF_C
7	SU3_PHA_IS	8	SU3_PHB_IS
9	SU3_PHC_IS	10	SU3_I_S_DCB
11	GND	12	+5.0V
13	NC	14	NC

2.13 General Purpose Switches and Run/Stop Switch

Two general-purpose user push button switches are connected to Port D GPIO signals, PD3 and PD4. A Run/Stop toggle switch is connected to GPIO signal PD5. Refer to [Figure 2-9](#).

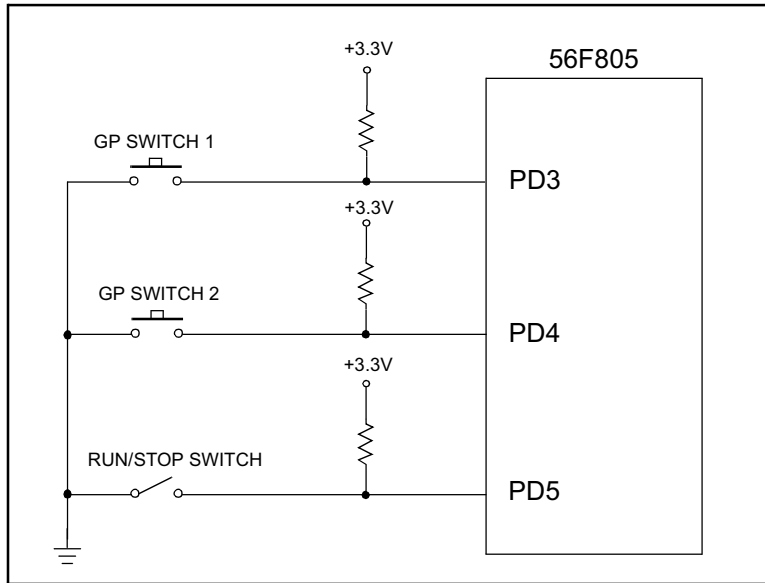


Figure 2-9. Run/Stop and General Purpose Switches

2.14 Serial 10-bit 4-channel D/A Converter

The 56F805EVM board contains a serial 10-bit, 4-channel D/A converter connected to the 56F805's SPI port. The output pins are uncommitted and are connected to a 4X2 header, J20, to allow easy user connections. Refer to [Figure 2-10](#) for the D/A connections and to [Table 2-10](#) for the header's pin out. The D/A's output full-scale range value can be set to a value from 0.0V to 2.4V by a trimpot. This trimpot is preset to 2.05V, which provides approximately 2mV per step.

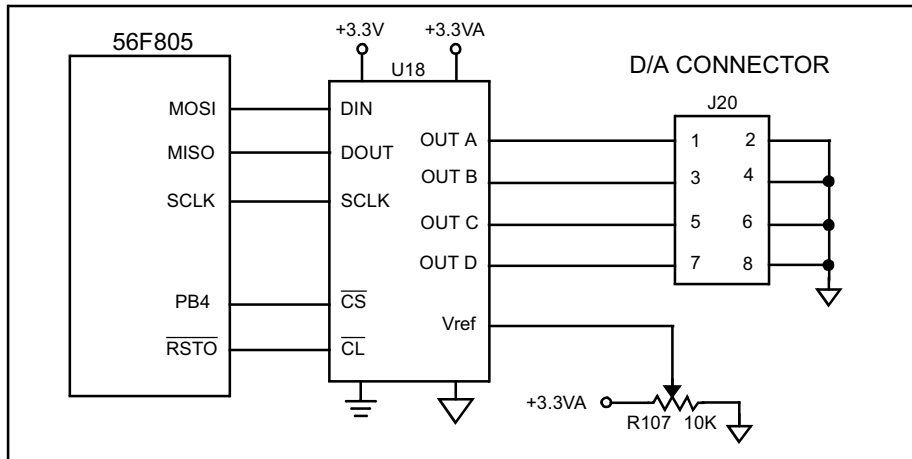


Figure 2-10. Serial 10-bit, 4-Channel D/A Converter

Table 2-10. D/A Header Description

J20			
Pin #	Signal	Pin #	Signal
1	D/A Channel 0	2	AGND
3	D/A Channel 1	4	AGND
5	D/A Channel 2	6	AGND
7	D/A Channel 3	8	AGND

2.15 Motor Control PWM Signals and LEDs

The 56F805 has two independent groups of dedicated PWM units. Each unit contains six PWM, three Phase Current sense and four Fault input lines. PWM group A's PWM lines are connected to the UNI-3 interface connector and to a set of six PWM LEDs via inverting buffers. The buffers are used to isolate and drive the controller's PWM outputs to the PWM LEDs. Most of the secondary PWM signals are routed to the Secondary UNI-3 connector. The PWM LEDs indicate the status of PWM group A signals; as shown in [Figure 2-11](#). PWM Group A and B signals are routed out to headers and are available for use by the end user.

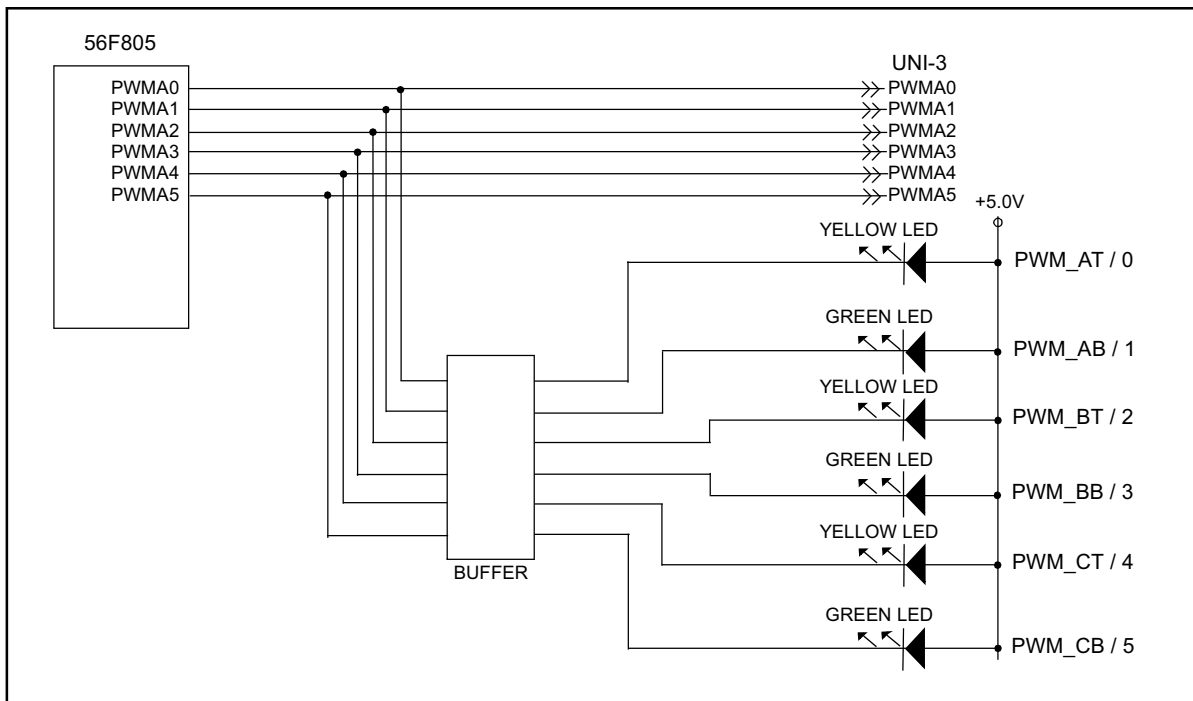


Figure 2-11. PWM Group A Interface and LEDs

2.16 Motor Protection Logic

The 56F805EVM contains two UNI-3 connectors that interface with various motor drive boards, Primary UNI-3 and Secondary UNI-3. The device can sense error conditions generated by the motor power stage boards via signals on the UNI-3 connector. The motor driver board's Motor Supply DC Bus Voltage, Current and Motor Phase Currents are sensed on the power stage board. The conditioned signals are transferred to the board via the UNI-3 connector. These analog input signals are compared to a limit set by trim pots. If the input analog signals are greater than the limit set by the trim pot, a controller digital voltage-compatible +3.3V DC fault signal is generated.

2.16.1 Primary UNI-3 Motor Protection Logic

The Primary UNI-3 DC Bus Over-Voltage signal is connected to the controller's PWM group A fault inputs. The three Primary UNI-3 Phase Over-Current signals are connected to the device's PWM group A's fault inputs, i.e., FAULTA1, FAULTA2 and FAULTA3. Figure 2-13 contains the diagram of the Over-Voltage and one phase of the Phase Over-Current circuit for the UNI-3 interface. The FAULTA1 input can be sourced from the Phase A Over-Current circuit or the DC Bus Over-Current circuit. Jumper JG15 provides the selection; see Figure 2-12 and Table 2-11.

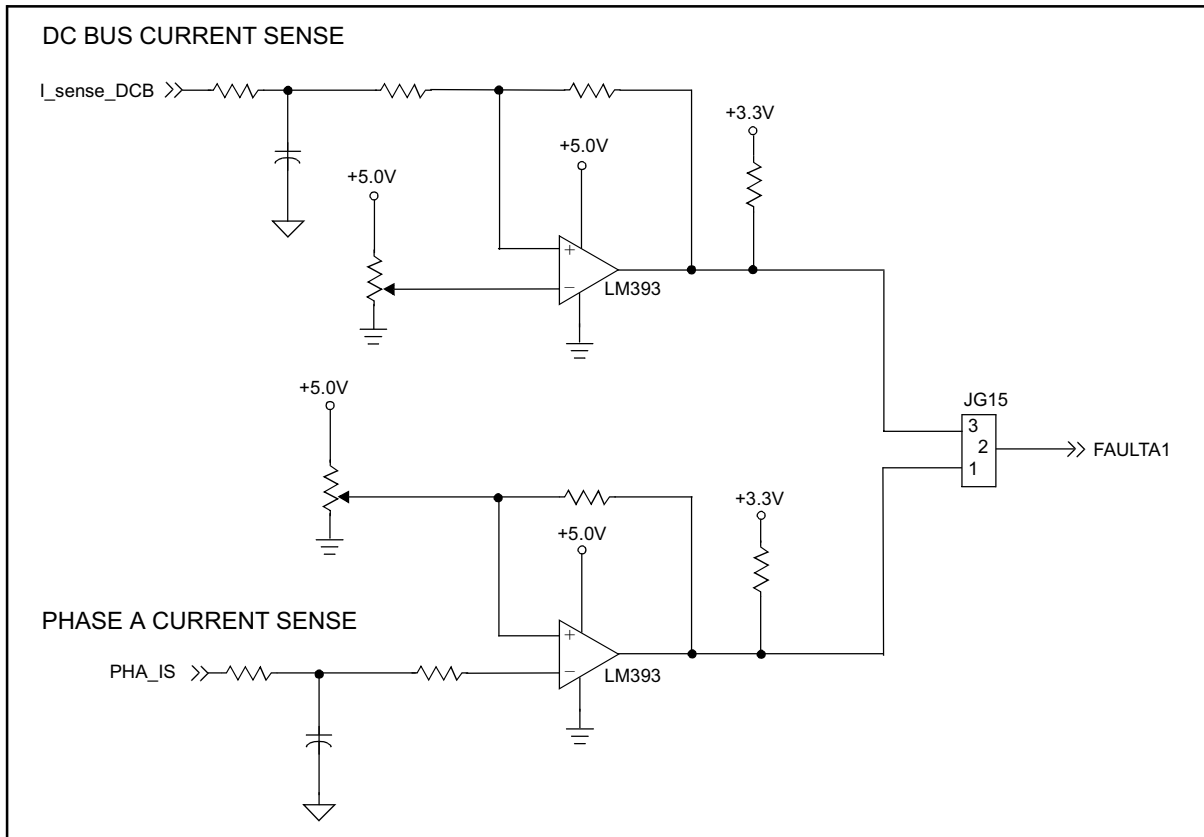


Figure 2-12. FAULTA1 Selection Circuit

Table 2-11. FAULTA1 Source Selection Jumper

JG15	Comment
1-2	Phase A Over-Current Sense input
2-3	DC Bus Over-Current Sense input

2.16.2 Secondary UNI-3 Motor Protection Logic

The Secondary UNI-3 interface is similar to the Primary UNI-3 interface. The Secondary UNI-3 Over-Voltage signal is connected to the controller's PWM group B's fault input, device's FAULTB0. The three Secondary UNI-3 Phase Over-Current signals are connected to the controller's PWM group B fault inputs, i.e., FAULTB1, FAULTB2 and FAULTB3. The Secondary UNI-3 interface is similar to the circuits contained in [Figure 2-13](#). The FAULTB1 input can be sourced from the Phase A Over-Current circuit or the DC Bus Over-Current circuit. Jumper JG16 provides the selection; reference [Figure 2-14](#) and [Table 2-12](#).

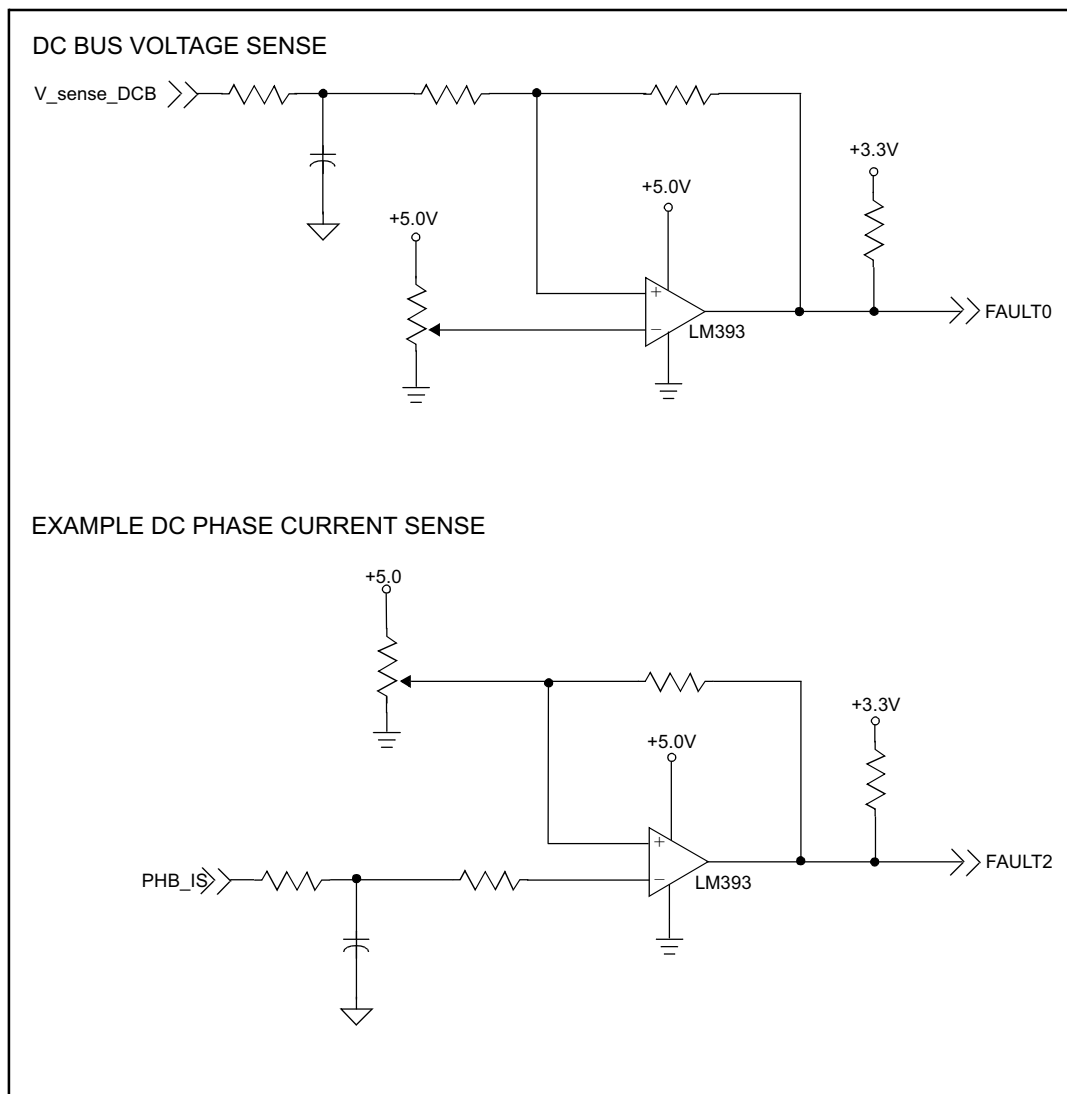


Figure 2-13. DC-Bus Over-Voltage and Phase Over-Current Detection Circuits

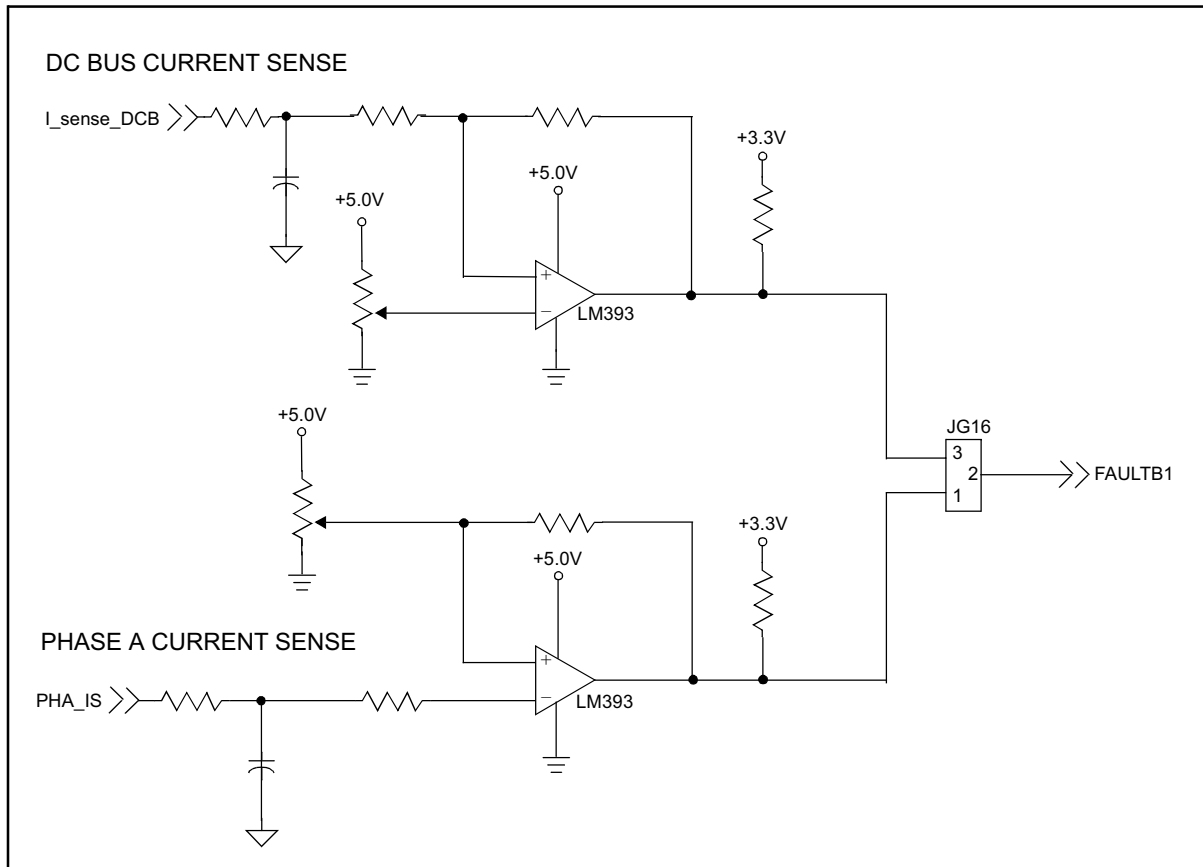


Figure 2-14. FAULTB1 Selection Circuit

Table 2-12. FAULTB1 Source Selection Jumper

JG16	Comment
1-2	Phase A Over-Current Sense input
2-3	DC Bus Over-Current Sense input

2.17 Back-EMF and Motor Phase Current Sensing

The primary and secondary UNI-3 connectors supply Back-EMF and Motor Phase Current signals from the three phases of a motor attached to a motor drive unit. The Back-EMF signals on the UNI-3 connectors are derived from a resistor divider network contained in the motor drive unit. These resistors divide down the attached motor's Back-EMF voltages to a 0 to +3.3V level. In certain instances the Back-EMF signals can exceed this maximum range. The Motor Phase Current signals are derived from current sense resistors. Both of these signal groups are then routed to a group of header pins that allow the end user to select which signal group the device's A/D will monitor. Refer to [Figure 2-15](#) for the design of a single channel. The Secondary UNI-3's Back-EMF signals are unbuffered and then routed to a header that contains all of the unconnected Secondary UNI-3 signals; reference [Table 2-9](#).

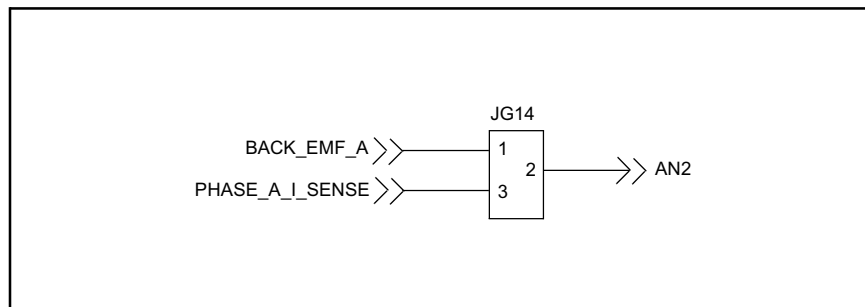


Figure 2-15. Primary Back-EMF or Motor Phase Current Sense Signals

2.18 Quadrature Encoder/Hall-Effect Interface

The 56F805EVM board contains a Primary and Secondary Quadrature Encoder/Hall-Effect interface connected to the controller's first and second Quad Encoder input ports. The circuit is designed to accept +3.0V to +5.0V encoder or Hall-Effect sensor inputs. Input noise filtering is supplied on the input path for the Quadrature Encoder/Hall-Effect interface, along with additional noise rejection circuitry inside the device. [Figure 2-16](#) contains the primary encoder interface. The secondary encoder interface is a duplicate of the primary encoder interface.

2.19 Zero-Crossing Detection

An attached UNI-3 motor drive board contains logic that can send out pulses when the phase voltage of an attached 3-phase motor drops to zero. The motor drive board circuits generate a 0 to +3.3V DC pulse via voltage comparators. The resulting pulse signals are sent to a set of jumper blocks shared with the Encoder/Hall-Effect interface. The jumper blocks allow the selection of Zero-Crossing signals or Quadrature Encoder/Hall-Effect signals. When in operation, the controller will only monitor one set of signals, Encoder/Hall-Effect or Zero-Crossing. [Figure 2-16](#) contains the Zero-Crossing and Encoder/Hall circuits.

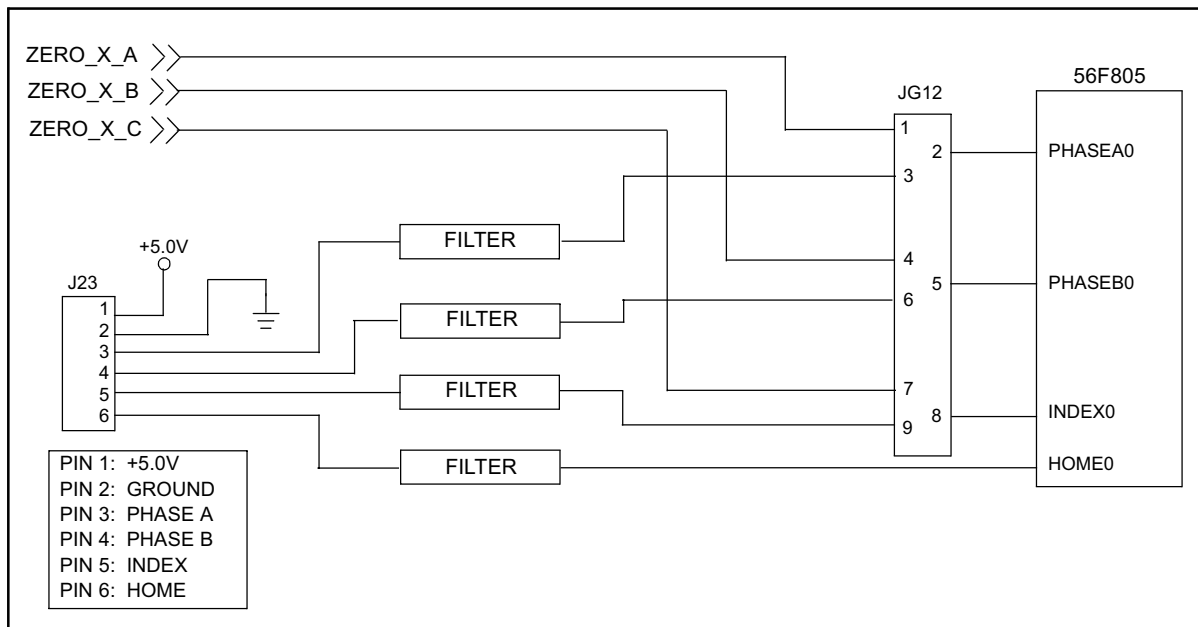


Figure 2-16. Zero-Crossing Encoder Interface

2.20 CAN Interface

The 56F805EVM board contains a CAN physical-layer interface chip that is attached to the MSCAN_RX and MSCAN_TX pins on the 56F805. The EVM board uses a Philips PCA82C250, high speed, 1Mbps, physical layer interface chip. Due to the +5.0V operating voltage of the CAN chip, a pull-up to +5.0V is required to level shift the Transmit Data output line from the 56F805. A primary, J26, and daisy-chain, J32, CAN connector are provided to allow easy daisy-chaining of CAN devices. CAN bus termination of 120 ohms can be provided by adding a jumper to JG17. Refer to [Table 2-13](#) for the CAN connector signals and [Figure 2-17](#) for a connection diagram.

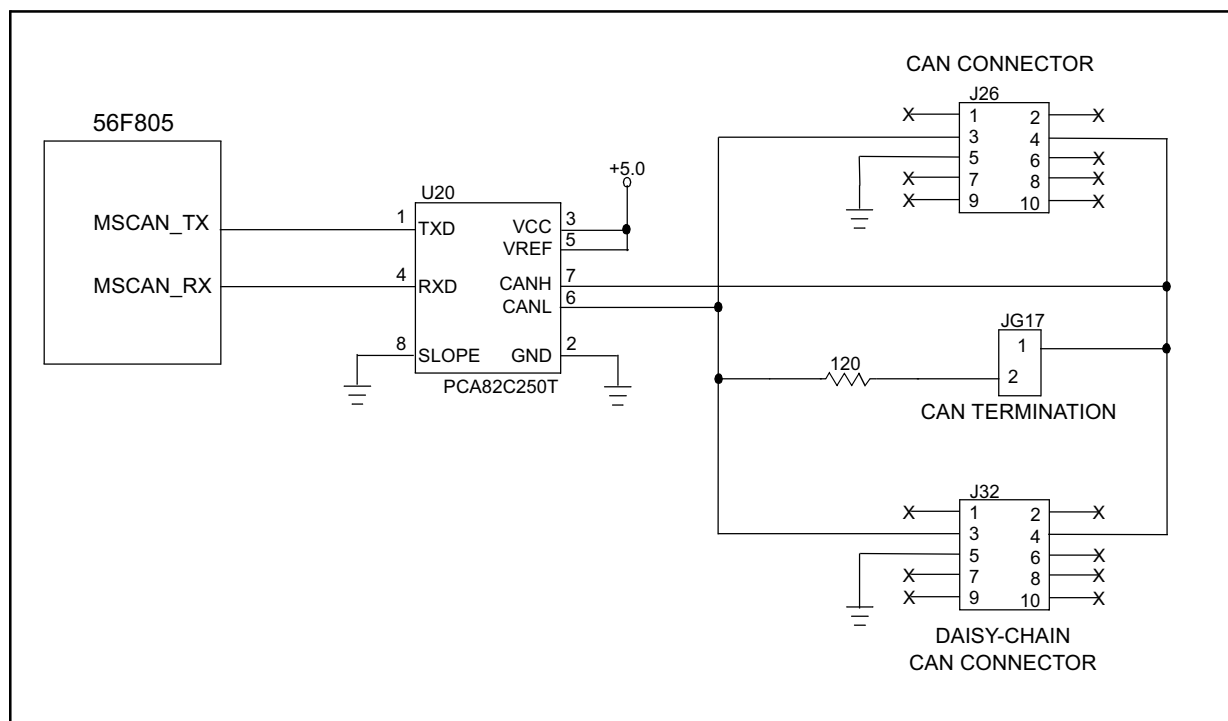


Figure 2-17. CAN Interface

Table 2-13. CAN Header Description

J26 and J32			
Pin #	Signal	Pin #	Signal
1	NC	2	NC
3	CANL	4	CANH
5	GND	6	NC
7	NC	8	NC
9	NC	10	NC

2.21 Software Feature Jumpers

The 56F805EVM board contains two software feature jumpers that allow the user to select “User Defined” software features. Two GPIO port pins, PD0 and PD1, are pulled high with 10k ohm resistors on JG1 and JG2. Attaching a jumper will ground the respective Port D signal line; see [Figure 2-18](#).

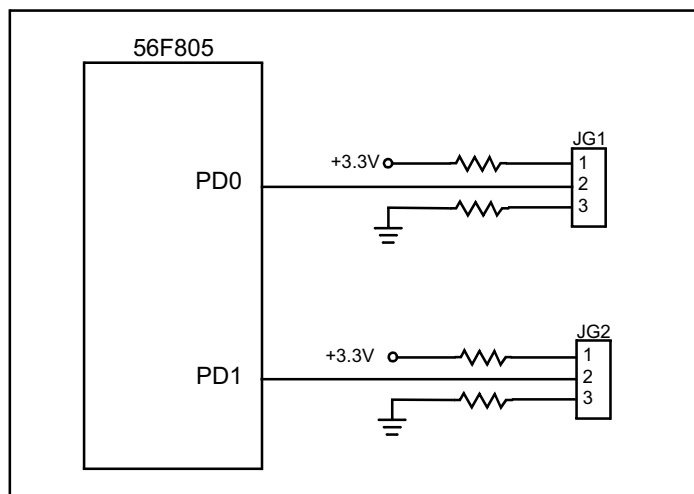


Figure 2-18. Software Feature Jumpers

2.22 Peripheral Connectors

The EVM board contains a group of Peripheral Expansion Connectors used to gain access to the resources of the 56F805. The following signal groups have Expansion Connectors:

- Port B
- Port D
- Port E
- External Memory Control
- Encoder A/Timer Channel A
- Encoder B/Timer Channel B
- Timer Channel C
- Timer Channel D
- Port A/Address Bus
- Data Bus
- A/D Input Port
- Serial Communications Port 0
- Serial Communications Port 1
- Serial Peripheral Port
- PWM Port A
- PWM Port B

2.22.1 Port B Expansion Connector

Port B is a GPIO port which is connected to the Port B header. The pins of the port, PB0-PB7, are dedicated to general purpose I/O and Interrupt operations. The GPIO port pins may be programmed as inputs, outputs or level-sensitive interrupt inputs. [Table 2-14](#) shows the port pin to headed connections.

Table 2-14. Port B Connector Description

J28			
Pin #	Signal	Pin #	Signal
1	PB0	2	PB1
3	PB2	4	PB3
5	PB4	6	PB5
7	PB6	8	PB7
9	GND	10	+3.3V

2.22.2 Port D Expansion Connector

Port D is an MPIO port with signal lines attached to various headers. The six pins of the port, PD0-PD5, are dedicated to general purpose operation. The remaining two pins, PD6 and PD7, are shared with the TXD1 and RXD1 signal lines. The GPIO port pins may be programmed as inputs, outputs or level-sensitive interrupt inputs. [Table 2-15](#) shows the exclusive Port D signals. The shared Port D signals are contained in [Table 2-22](#).

Table 2-15. Port D Connector Description

J4			
Pin #	Signal	Pin #	Signal
1	PD0	2	PD1
3	PD2	4	PD3
5	PD4	6	PD5
7	GND	8	+3.3V

2.22.3 Port E Expansion Connector

Port E is an MPIO port with signal lines attached to various headers. The pins of the port are shared with one SCI port, SCI0, two Address bus lines, A6 and A7, and the SPI port. [Table 2-16](#) shows the shared pins and functions.

Table 2-16. Port E Connector Description

J7					
Pin #	Signal	Alternate Funct	Pin #	Signal	Alternate Funct
1	PE0	TXD0	2	PE1	RXD0
3	PE2	TXD1	4	PE3	RXD1
5	PE4	SCLK	6	PE5	MOSI
7	PE6	MISO	8	PE7	\overline{SS}
9	GND	GND	10	+3.3V	+3.3V

2.22.4 External Memory Control Signal Expansion Connector

The External Memory Control Signal connector contains the controller's external memory control signal lines. Refer to [Table 2-17](#) for the names of these signals.

Table 2-17. External Memory Control Signal Connector Description

J27			
Pin #	Signal	Pin #	Signal
1	\overline{RD}	2	\overline{IRQA}
3	\overline{WR}	4	\overline{IRQB}
5	\overline{PS}	6	\overline{RESET}
7	\overline{DS}	8	\overline{RSTO}
9	CLKO	10	DE
11	GND	12	+3.3V

2.22.5 Primary Encoder/Timer Channel A Expansion Connector

The Primary Encoder/Timer Channel A port is an MPIO port attached to the Timer A expansion connector. The port can act as a Quadrature Decoder interface port or as a general purpose Timer port. See to [Table 2-18](#) for the signals attached to the connector.

Table 2-18. Timer A Connector Description

J3		
Pin #	Signal	Alternate
1	TA0	PhaseA0
2	TA1	PhaseB0
3	TA2	INDEX0
4	TA3	HOME0
5	+3.3V	+3.3V
6	GND	GND

2.22.6 Secondary Encoder/Timer Channel B Expansion Connector

The Secondary Encoder/Timer Channel B port is an MPIO port attached to the Timer B expansion connector. The port can act as a Quadrature Decoder interface port or as a general purpose Timer port. Refer to [Table 2-19](#) for the signals attached to the connector.

Table 2-19. Timer B Connector Description

J6		
Pin #	Signal	Alternate
1	TB0	PhaseA1
2	TB1	PhaseB1
3	TB2	INDEX1
4	TB3	HOME1
5	+3.3V	+3.3V
6	GND	GND

2.22.7 Timer Channel C Expansion Connector

The Timer Channel C port is an MPIO port attached to the Timer C expansion connector. Refer to [Table 2-20](#) for the signals attached to the connector.

Table 2-20. Timer C Connector Description

J8	
Pin #	Signal
1	TC0
2	TC1
3	+3.3V
4	GND

2.22.8 Timer Channel D Expansion Connector

The Timer Channel D port is an MPIO port attached to the Timer D expansion connector. See [Table 2-21](#) for the signals attached to the connector.

Table 2-21. Timer D Connector Description

J5	
Pin #	Signal
1	TD0
2	TD1
3	TD2
4	TD3
5	+3.3V
6	GND

2.22.9 Address Bus Expansion Connector

The 16-bit Address bus connector contains the controller's external memory address signal lines. The upper 8 bits, A8 - A15, can also be used as Port A GPIO lines. Refer to [Table 2-22](#) for the Address bus connector information.

Table 2-22. External Memory Address Bus Connector Description

J1			
Pin #	Signal	Pin #	Signal
1	A0	2	A1
3	A2	4	A3
5	A4	6	A5
7	A6	8	A7
9	A8	10	A9
11	A10	12	A11
13	A12	14	A13
15	A14	16	A15
17	GND	18	+3.3V

2.22.10 Data Bus Expansion Connector

The 16-bit Data bus connector contains the controller's external memory data signal lines. Refer to [Table 2-23](#) for the Data bus connector information.

Table 2-23. External Memory Address Bus Connector Description

J2			
Pin #	Signal	Pin #	Signal
1	D0	2	D1
3	D2	4	D3
5	D4	6	D5
7	D6	8	D7
9	D8	10	D9
11	D10	12	D11
13	D12	14	D13
15	D14	16	D15
17	GND	18	+3.3V

2.22.11 A/D Port Expansion Connector

The 8-channel Analog-to-Digital conversion port is attached to this connector. See [Table 2-24](#) for connection information.

Table 2-24. A/D Connector Description

J9			
Pin #	Signal	Pin #	Signal
1	AN0	2	AN4
3	AN1	4	AN5
5	AN2	6	AN6
7	AN3	8	AN7
9	GND A	10	+3.3VA

2.22.12 Serial Communications Port 0 Expansion Connector

The Serial Communications Port 0, SCI0, is attached to this connector. Refer to [Table 2-25](#) for connection information.

Table 2-25. SCI0 Connector Description

J16	
Pin #	Signal
1	TXD0
2	RXD0
3	GND

2.22.13 Serial Communications Port 1 Expansion Connector

The Serial Communications Port 1, SCI1, is attached to this connector. Refer to [Table 2-26](#) for connection information.

Table 2-26. SCI1 Connector Description

J17	
Pin #	Signal
1	TXD1
2	RXD1
3	GND

2.22.14 Serial Peripheral Interface Expansion Connector

The Serial Peripheral Interface, SPI, is attached to this connector. Refer to [Table 2-27](#) for connection information.

Table 2-27. SPI Connector Description

J19	
Pin #	Signal
1	MOSI
2	MISO
3	SCLK
4	GND

2.22.15 CAN Expansion Connector

The CAN port is attached to this connector. Refer to [Table 2-28](#) for connection information.

Table 2-28. CAN Connector Description

J25	
Pin #	Signal
1	MSCAN_TX
2	MSCAN_RX
3	GND

2.22.16 PWM Port A Expansion Connector

The PWM port A is attached to this connector. Refer to [Table 2-29](#) for the connection information.

Table 2-29. PWM Port A Connector Description

J21	
Pin #	Signal
1	ISA0
2	ISA1
3	ISA2
4	FAULTA0
5	FAULTA1
6	FAULTA2
7	FAULTA3
8	PWMA0
9	PWMA1
10	PWMA2
11	PWMA3
12	PWMA4
13	PWMA5
14	GND

2.22.17 PWM Port B Expansion Connector

The PWM port B is attached to this connector. Refer to [Table 2-30](#) for the connection information.

Table 2-30. PWM Port B Connector Description

J22	
Pin #	Signal
1	ISB0
2	ISB1
3	ISB2
4	FAULTB0
5	FAULTB1
6	FAULTB2
7	FAULTB3
8	PWMB0
9	PWMB1
10	PWMB2
11	PWMB3
12	PWMB4
13	PWMB5
14	GND

2.23 Secondary UNI-3 Unattached Signal Connector

The Secondary UNI-3 signal group has several lines that do not connect to the controller. These unattached lines are connected to a header where they are available for use by the end user. Refer to [Table 2-31](#) for the location of these signals.

Table 2-31. Secondary UNI-3 Unattached Signal Connector Description

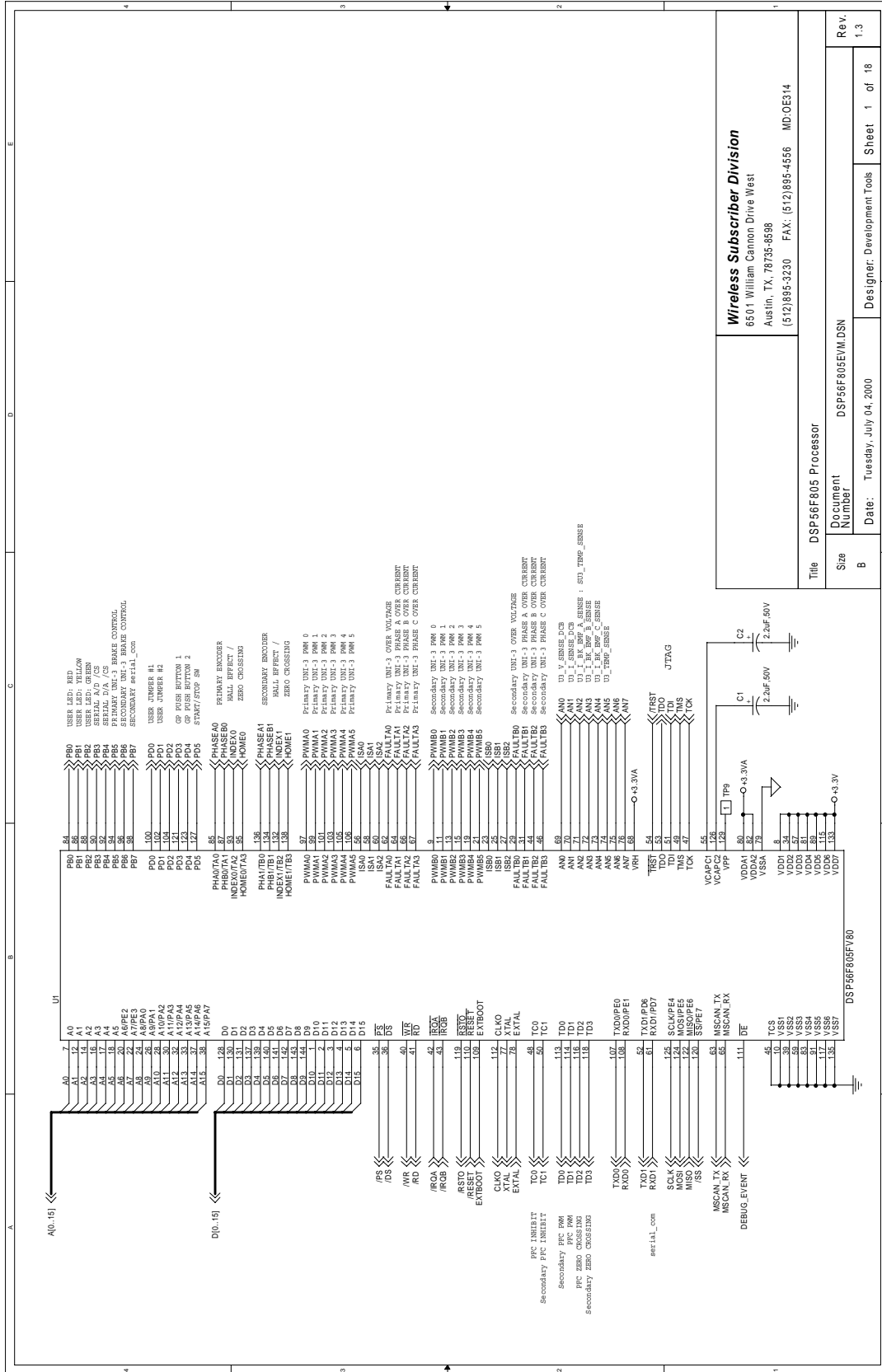
J14			
Pin #	Signal	Pin #	Signal
1	SU3_ZERO_X_A	2	SU3_ZERO_X_B
3	SU3_ZERO_X_C	4	SU3_BK_EMF_A
5	SU3_BK_EMF_B	6	SU3_BK_EMF_C
7	SU3_PHA_IS	8	SU3_PHB_IS
9	SU3_PHC_IS	10	SU3_I_S_DCB
11	GND	12	+5.0V
13	NC	14	NC

2.24 Test Points

The 56F805EVM board has a total of eight test points. Four test points are located near the breadboard area: +3.3VA, AGND, +3.3V and GND. Four test points are located near the Primary UNI-3 connector, J30: -15VA, GND, +15VA and GND.

Appendix A

56F805EVM Schematics



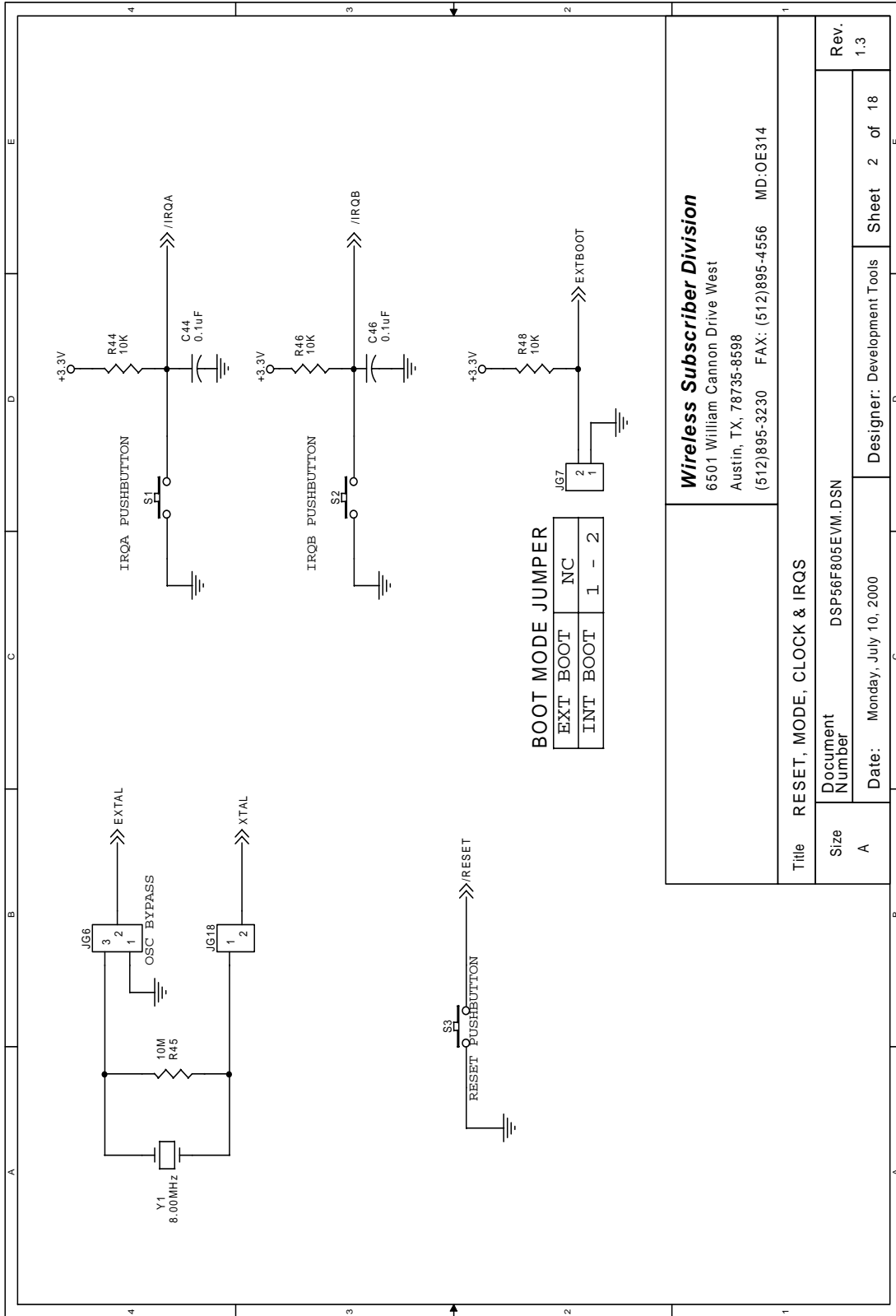
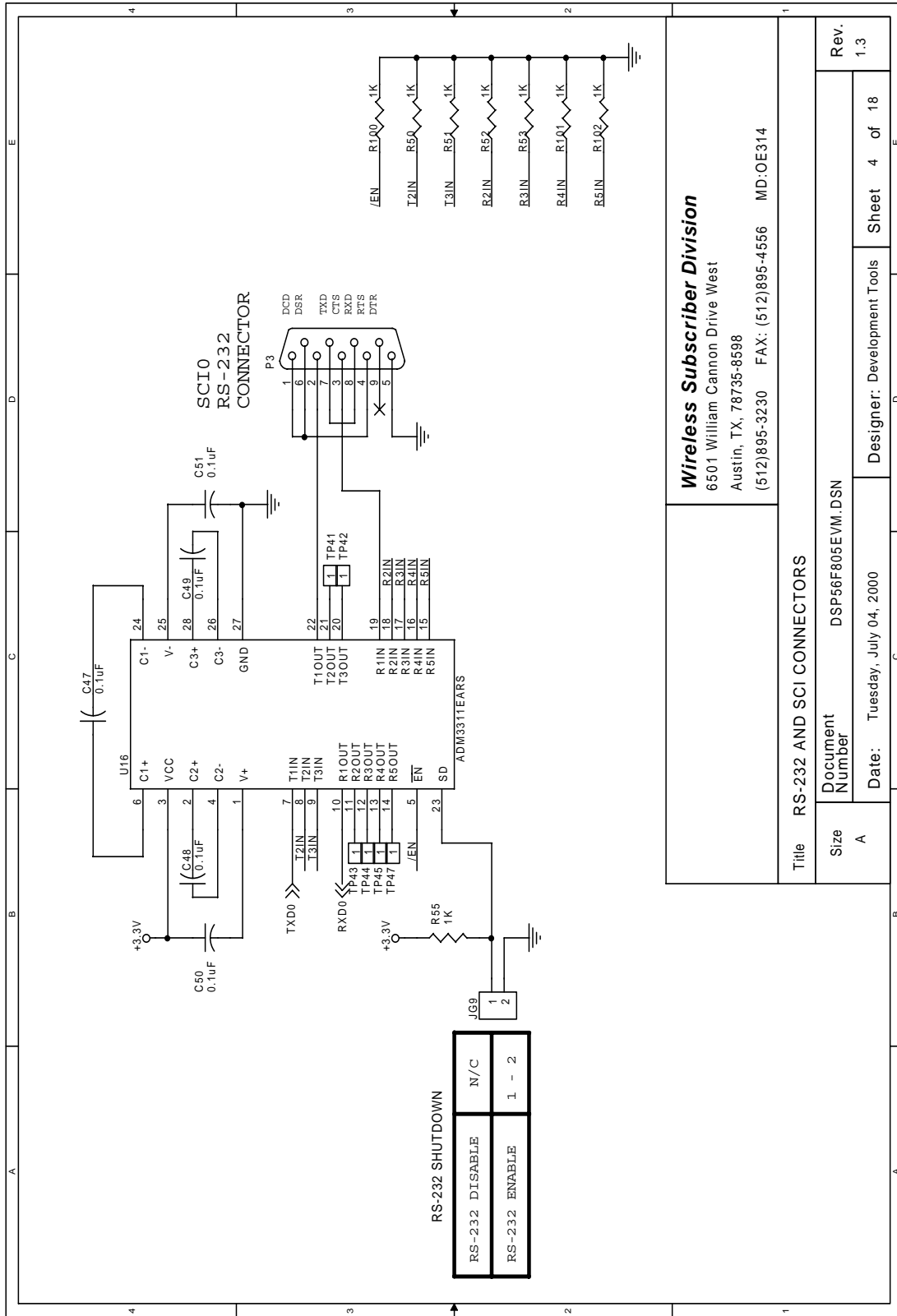
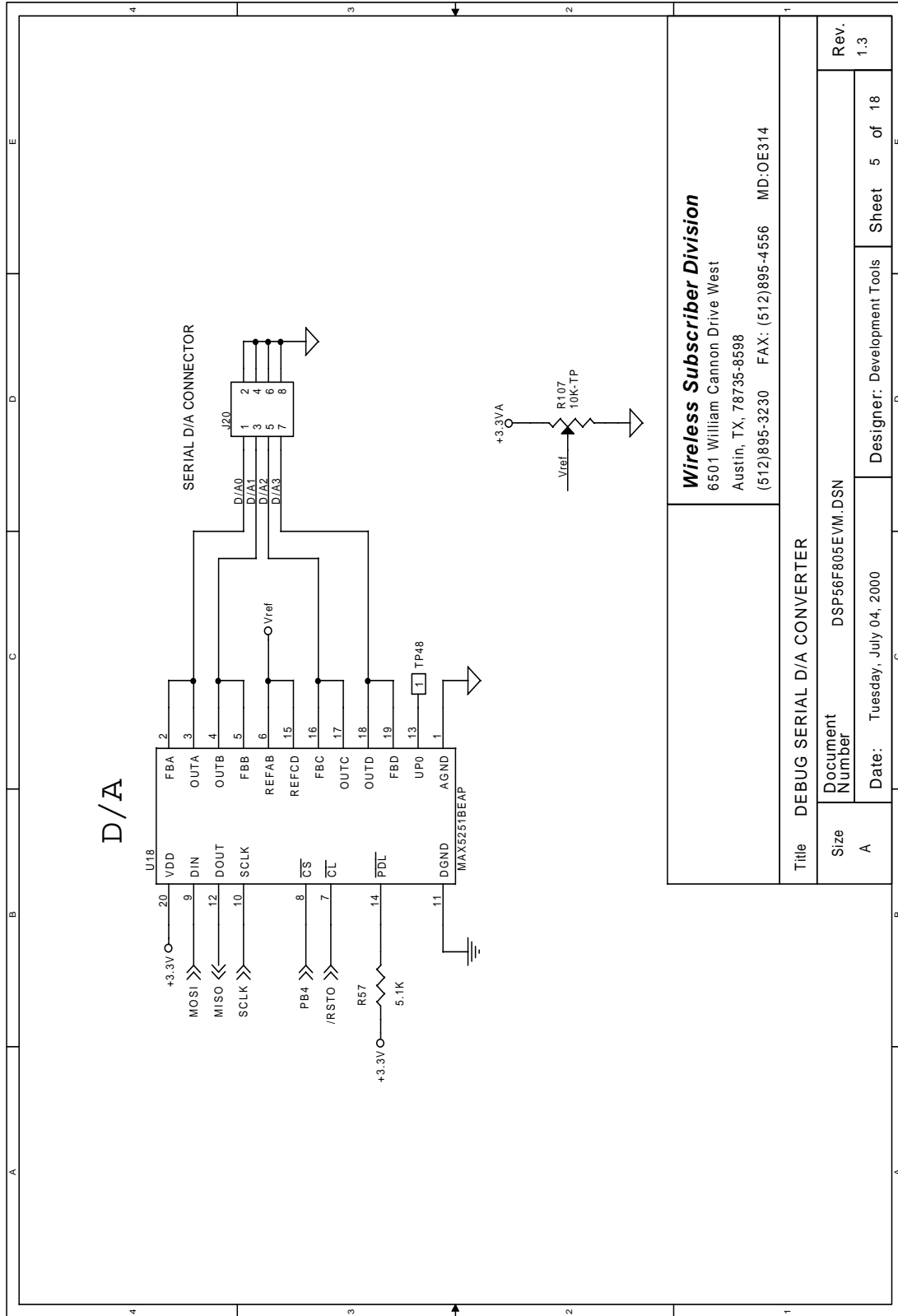


Figure A-2. Reset, Mode, Clock & IRQs



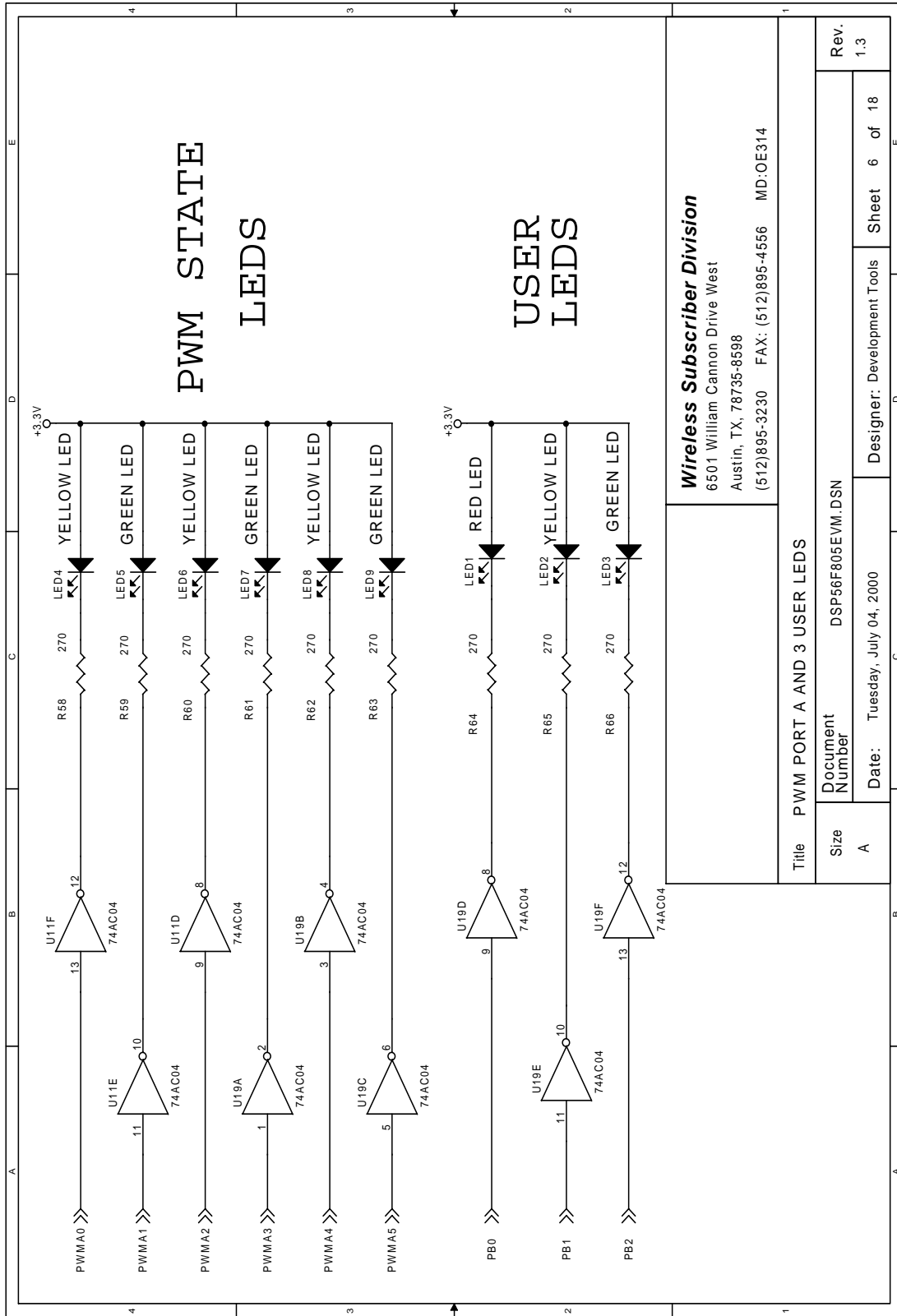
Wireless Subscriber Division	
6501 William Cannon Drive West Austin, TX, 78735-8598 (512)895-3230 FAX: (512)895-4556 MD:OE314	
Title RS-232 AND SCI CONNECTORS	
Document Number	DSP56F805EVM.DSN
Size	A
Date:	Tuesday, July 04, 2000
Designer:	Development Tools
Sheet	4 of 18
Rev.	1.3

Figure A-4. RS-232 and SCI Connectors



Wireless Subscriber Division		6501 William Cannon Drive West Austin, TX, 78735-8598 (512)895-3230 FAX: (512)895-4566 MD:OE314	
Title DEBUG SERIAL D/A CONVERTER			
Size	Document Number	Date	Rev.
A	DSP56F805EVM.DSN	Tuesday, July 04, 2000	1.3
		Designer: Development Tools	Sheet 5 of 18

Figure A-5. Debug Serial D/A Converter



Wireless Subscriber Division 6501 William Cannon Drive West Austin, TX, 78735-8598 (512)895-3230 FAX: (512)895-4556 MD:OE314		Title	
		PWM PORT A AND 3 USER LEDs	
Size	Document Number	Rev.	
A	DSP56F805EVM.DSN	1.3	
Date:	Designer:	Sheet	of
Tuesday, July 04, 2000	Development Tools	6	18

Figure A-6. PWM A AND Three User LEDs

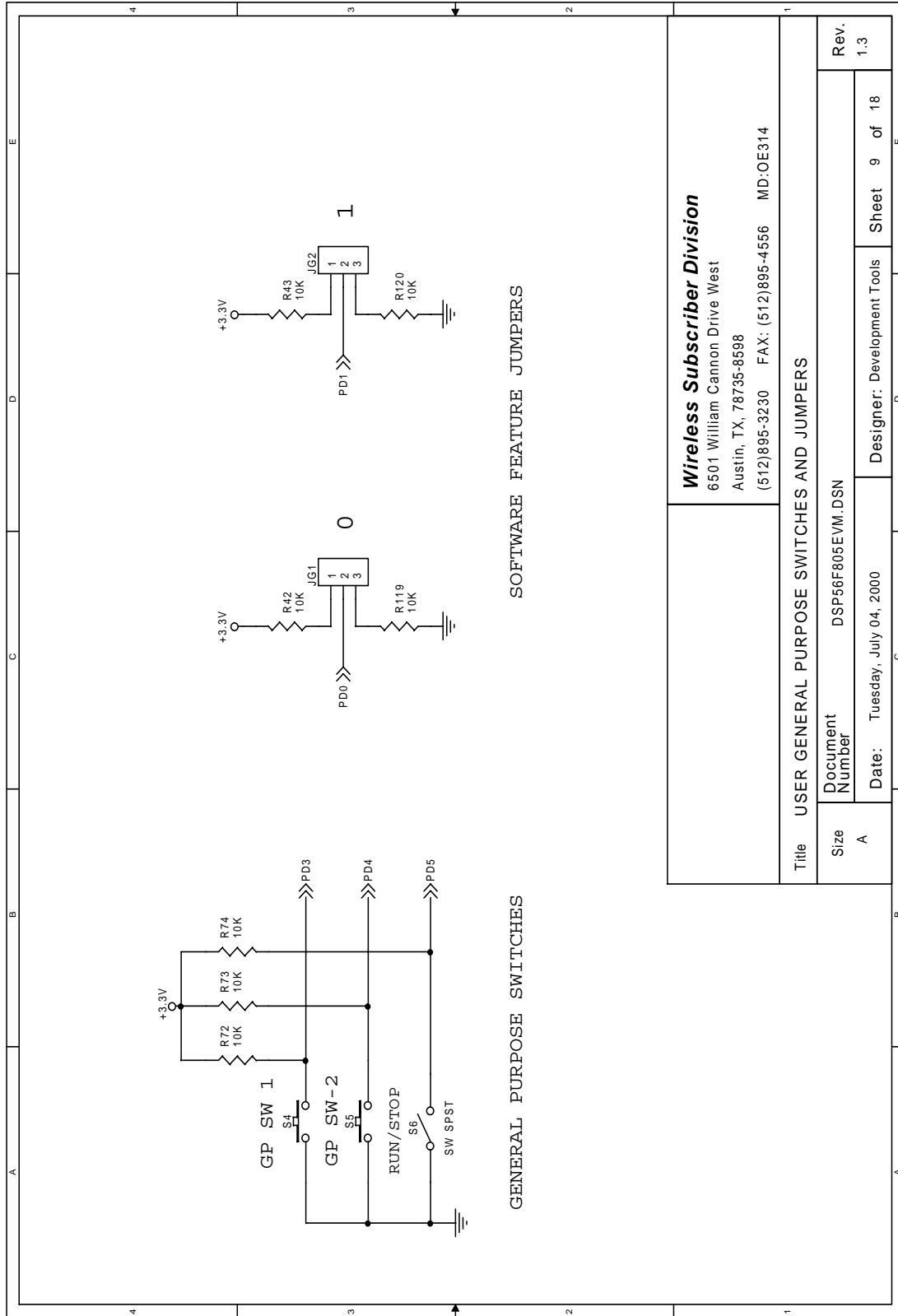


Figure A-9. User General Purpose Switches and Jumpers

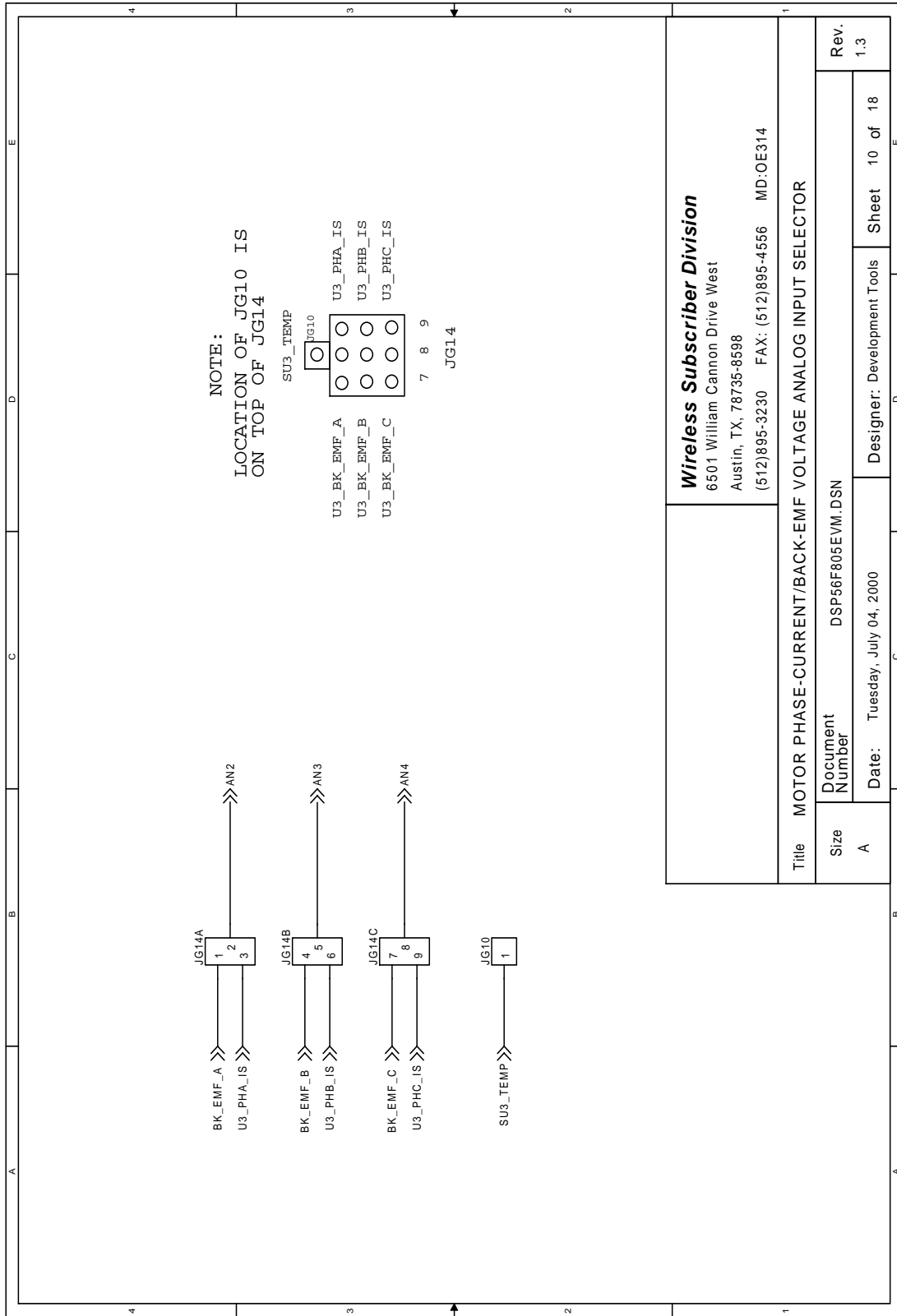
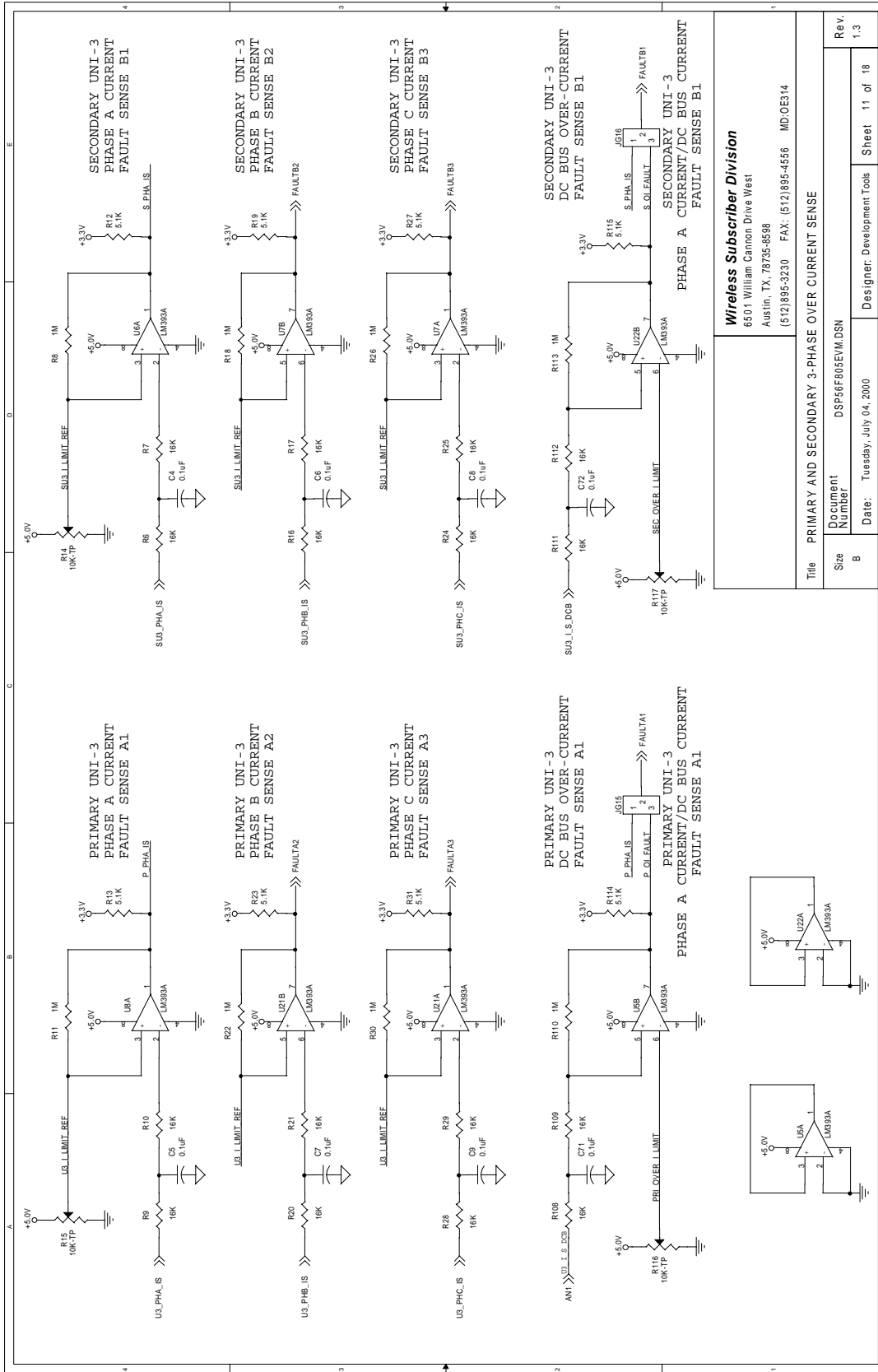


Figure A-10. Motor Phase-Current/Back-EMF Voltage Analog Input Selector



Wireless Subscriber Division 6501 William Cannon Drive West Austin, TX, 78735-6598 (512)895-3230 FAX: (512)895-4556 MD-0E314	
PRIMARY AND SECONDARY 3-PHASE OVER CURRENT SENSE	
Title Document Number Size B	DSP56F805EVM.DSN
Date: Tuesday, July 04, 2000	Designer: Development Tools
Rev. 1.3	Sheet 11 of 18

Figure A-11. Primary and Secondary 3-Phase Over-Current Sense

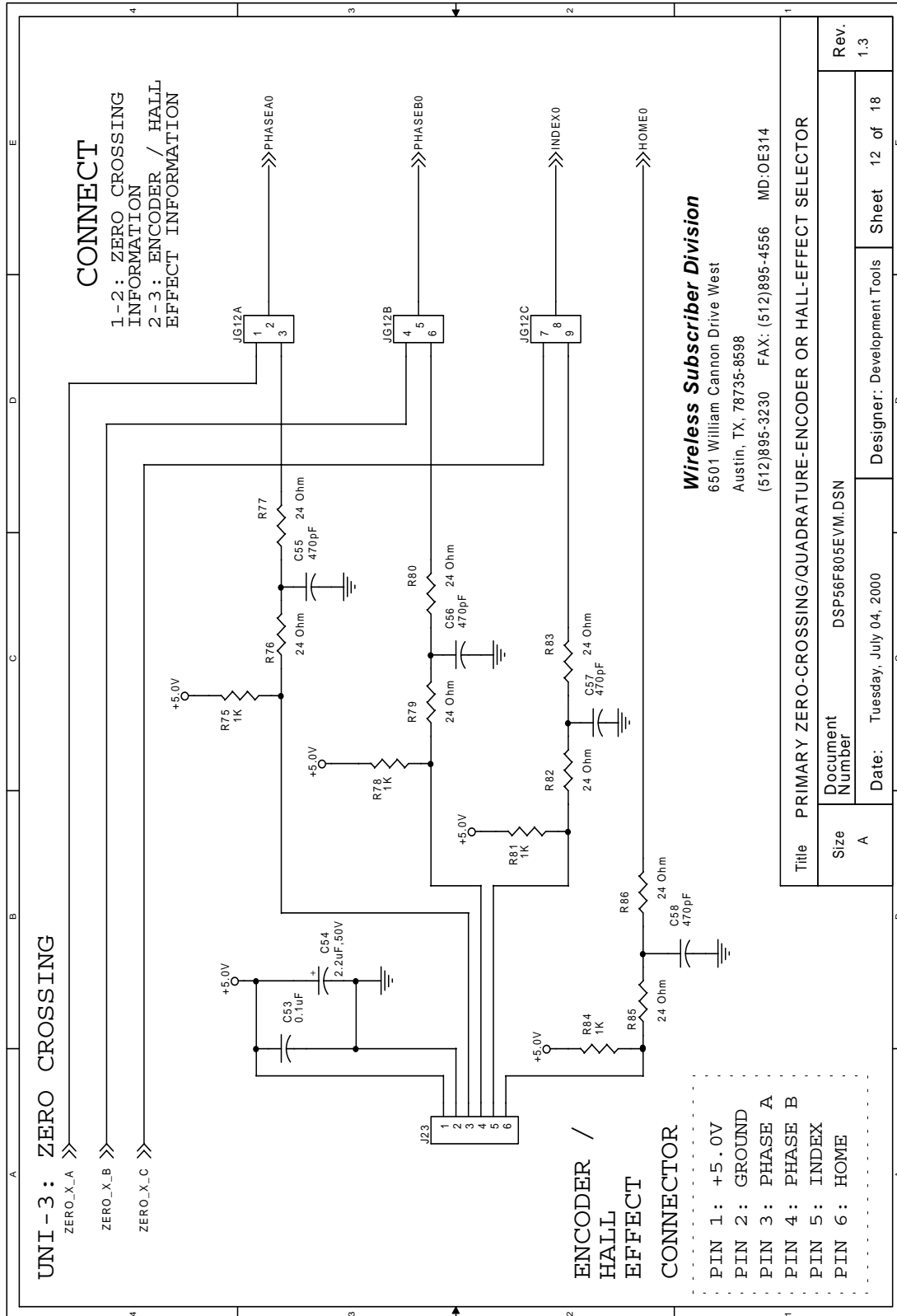


Figure A-12. Primary Zero-Crossing/Quadrature-Encoder or Hall-Effect Selector

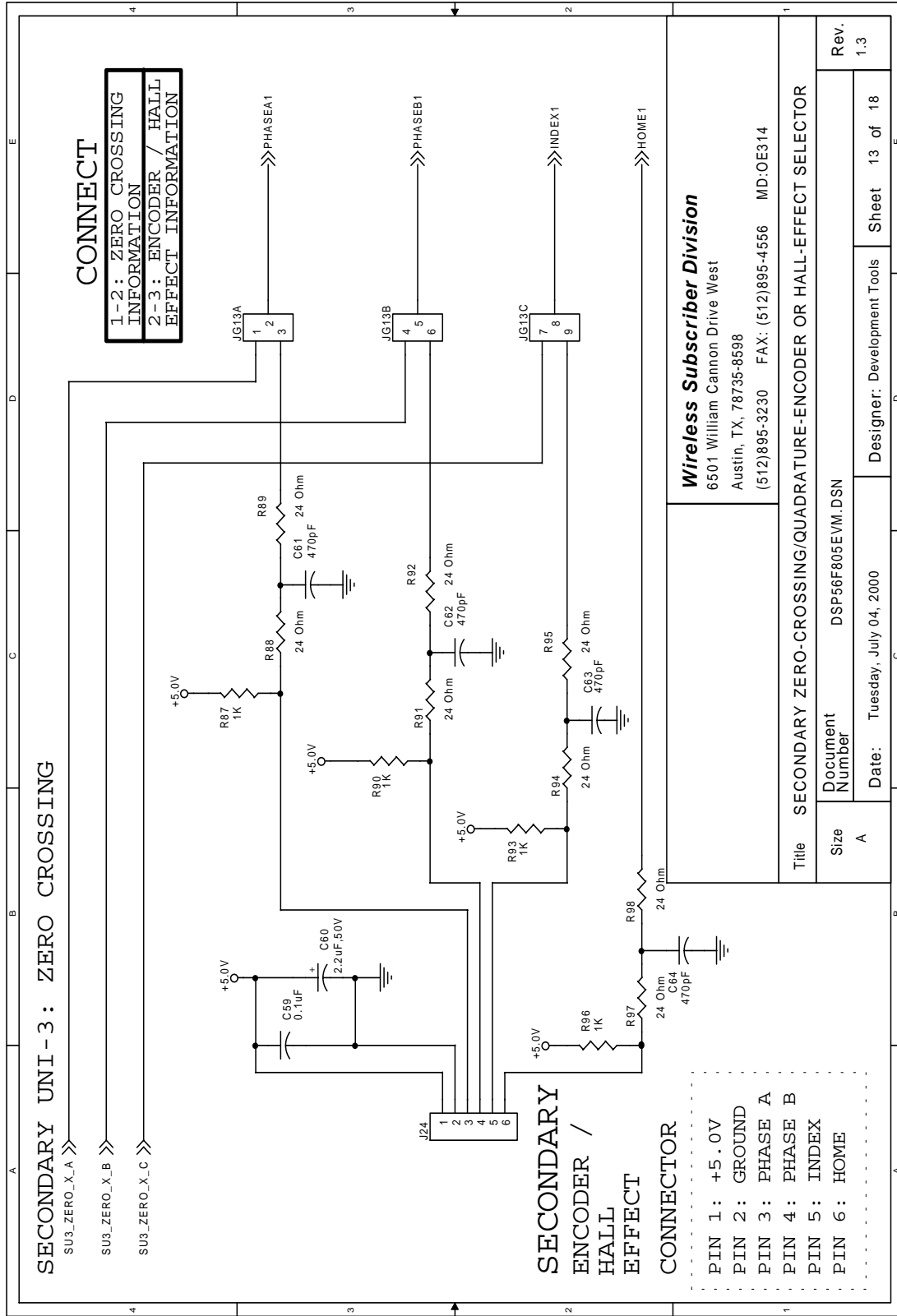


Figure A-13. Secondary Zero-Crossing/Quadrature-Encoder or Hall-Effect Selector

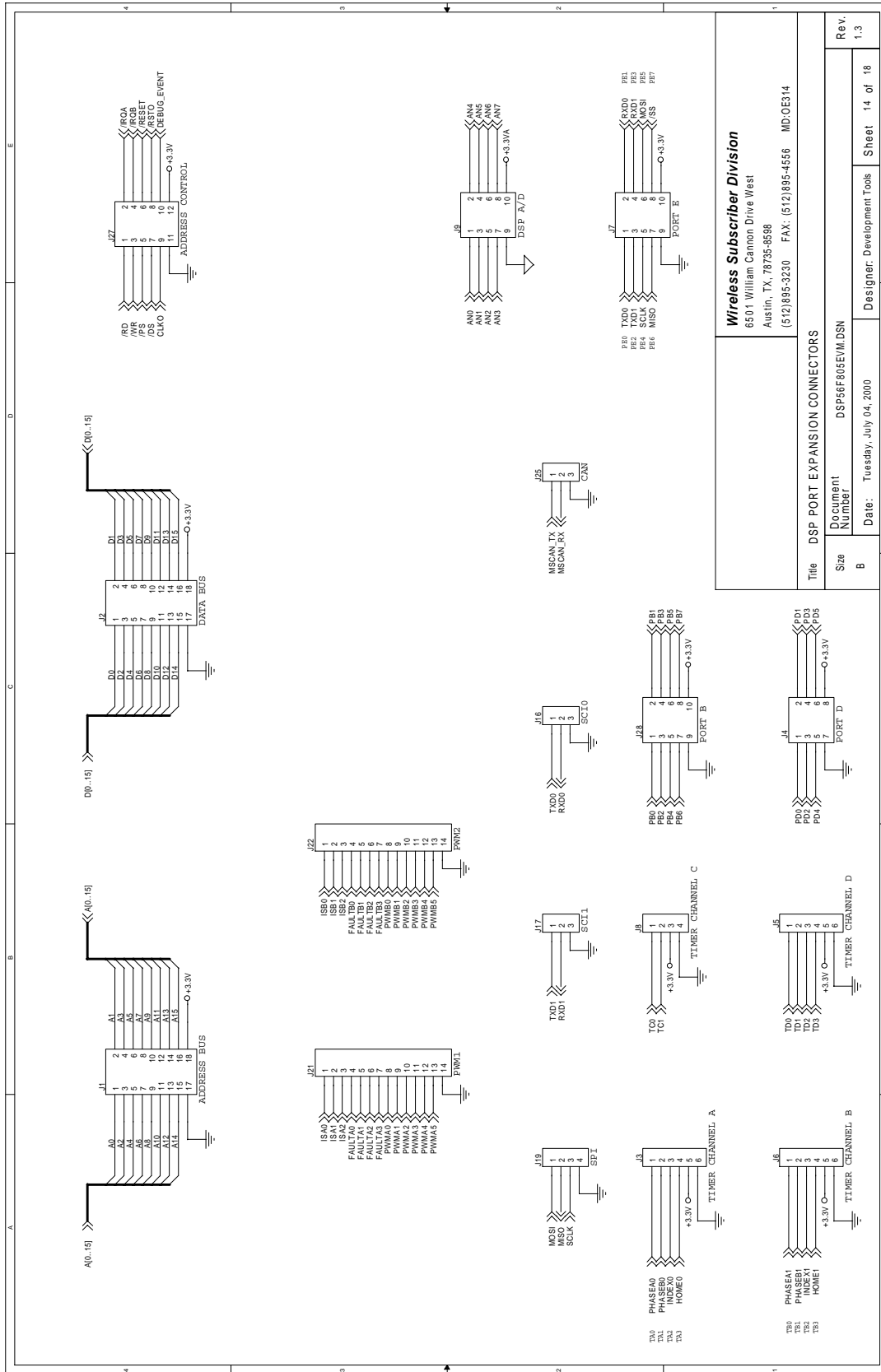
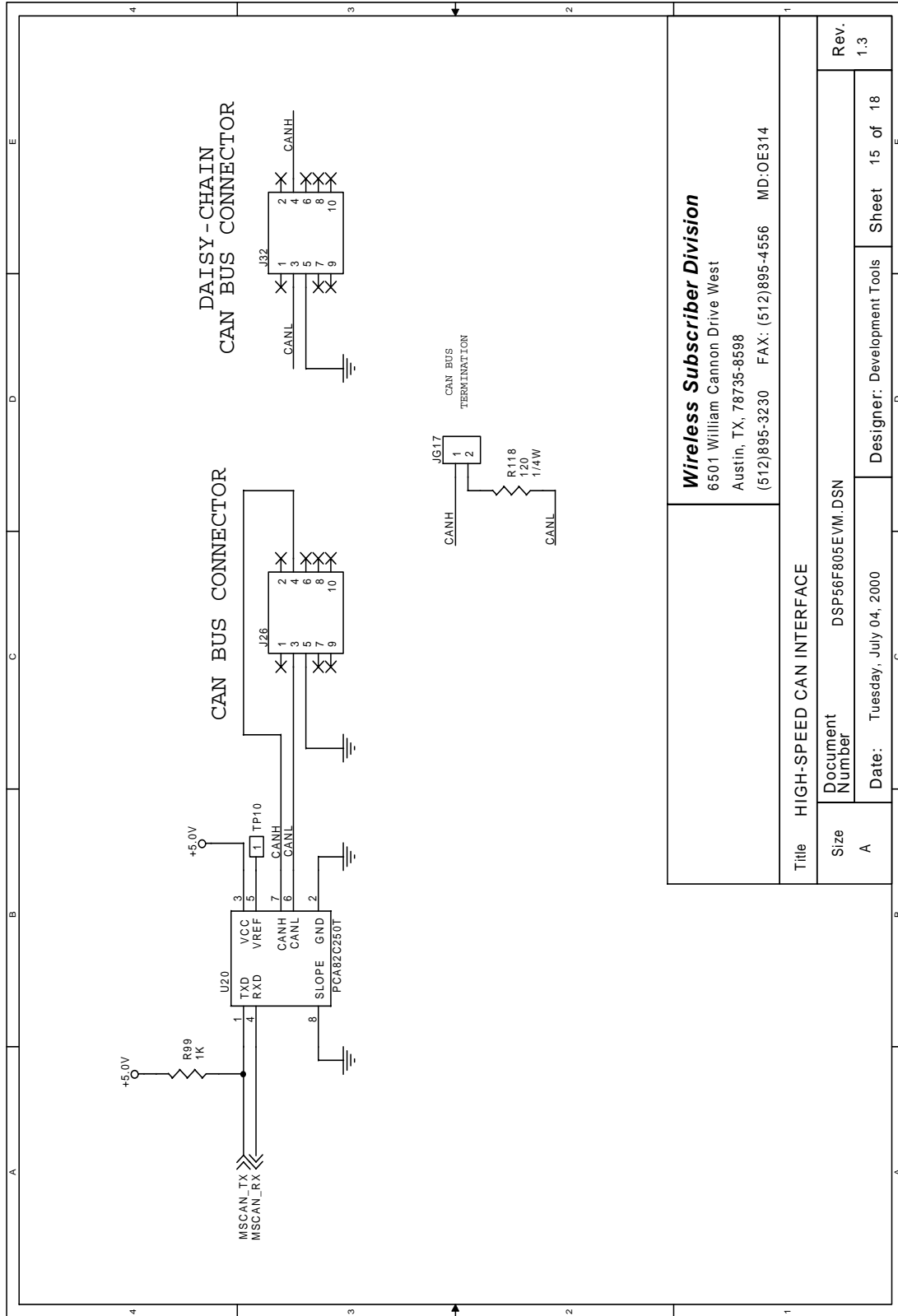


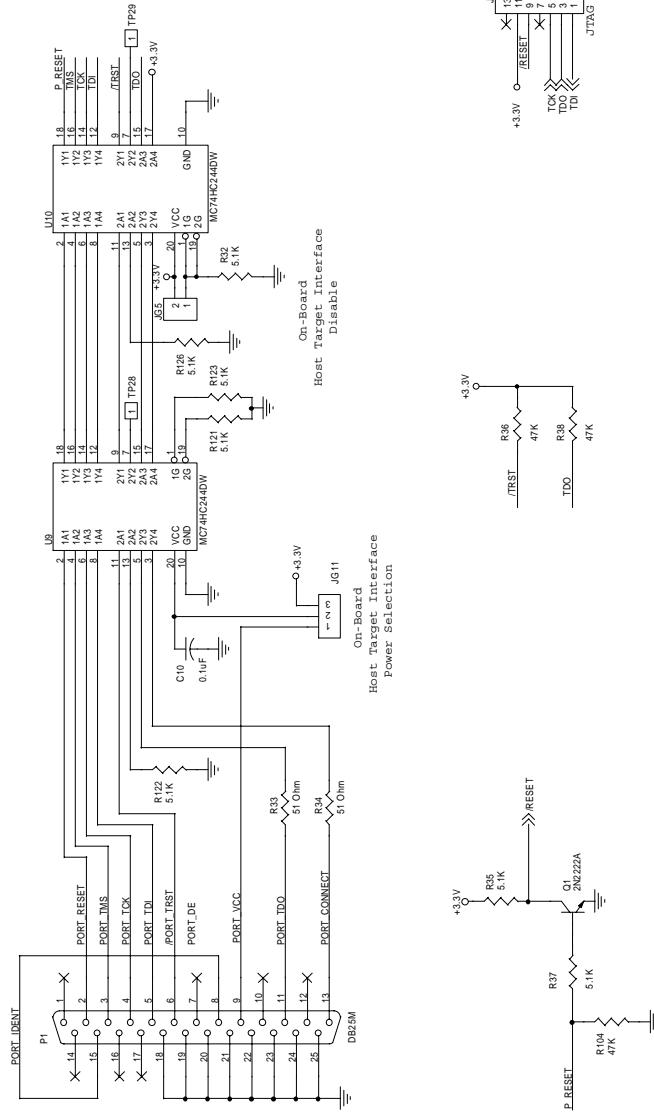
Figure A-14. Port Expansion Connectors



Wireless Subscriber Division 6501 William Cannon Drive West Austin, TX, 78735-8598 (512)895-3230 FAX: (512)895-4566 MD:OE314	
Title HIGH-SPEED CAN INTERFACE	
Size A	Document Number DSP56F805EVM.DSN
Date Tuesday, July 04, 2000	Designer: Development Tools
Sheet 15 of 18	Rev. 1.3

Figure A-15. High-Speed CAN Interface

Parallel JTAG Interface



Wireless Subscriber Division 6501 William Cannon Drive West Austin, TX, 78735-6598 (512)895-3230 FAX: (512)895-4556 MD,OE314	
PARALLEL JTAG HOST TARGET INTERFACE AND JTAG CONNECTOR	
Title Document Number Size B	DSP56F805EVM.DSN B
Date: Tuesday, July 04, 2000	Designer: Development Tools
Sheet 16 of 18	Rev. 1.3

Figure A-16. Parallel JTAG Host Target Interface and JTAG Connector

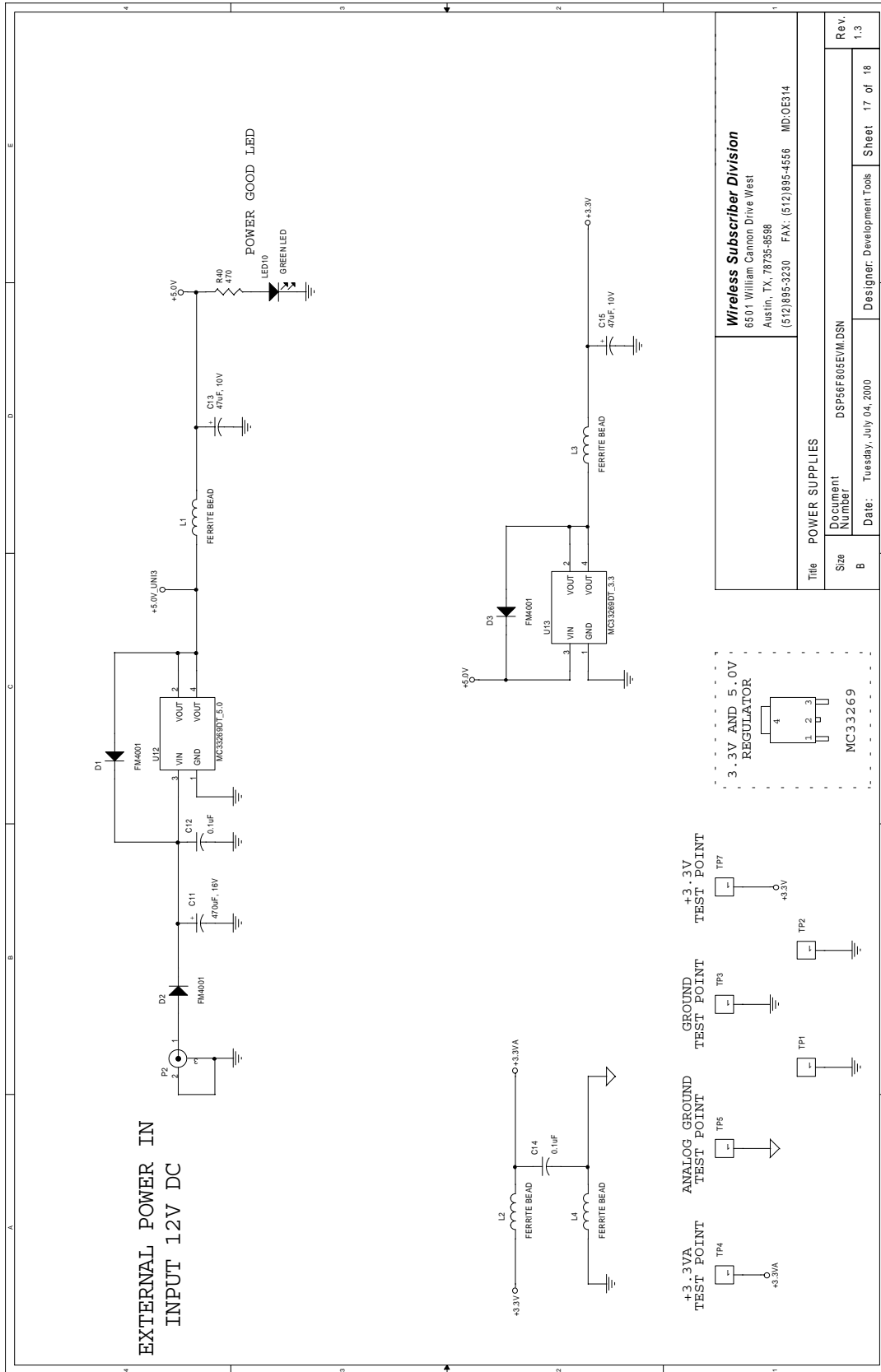
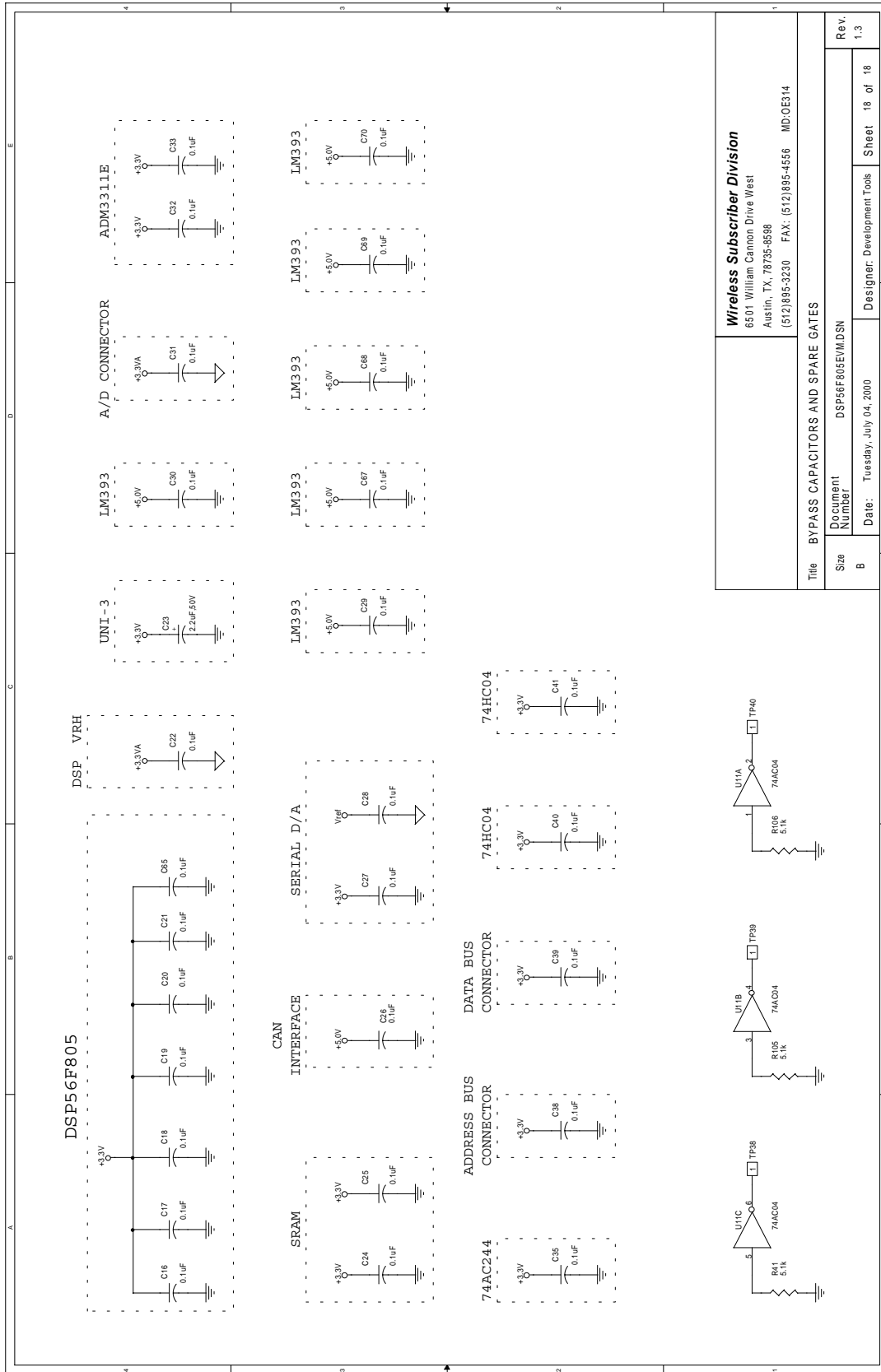


Figure A-17. Power Supplies



Wireless Subscriber Division 6501 William Cannon Drive West Austin, TX, 78735-8598 (512)895-3230 FAX: (512)895-4556 MD-CE314	
Title: BYPASS CAPACITORS AND SPARE GATES	
Document Number: DSP56F805EVM.DSN	Rev. 1.3
Date: Tuesday, July 04, 2000	Designer: Development Tools
Sheet 18 of 18	Sheet 18 of 18

Figure A-18. Bypass Capacitors and Spare Gates



Appendix B

56F805EVM Bill of Material

Qty	Description	Ref. Designators	Vendor Part #s
Integrated Circuits			
1	DSP56F805FV80	U1	Freescale, DSP56F805FV80
6	LM393M	U5, U6, U7, U8, U21, U22	National, LM393M
2	MC74HC244DW	U9, U10	ON Semiconductor, MC74HC244DW
2	74AC04SC	U11, U19	Fairchild, 74AC04SC
1	MC33269DT-5.0	U12	ON Semiconductor, MC33269DT-5.0
1	MC33269DT-3.3	U13	ON Semiconductor, MC33269DT-3.3
1	GS72116TP-12	U15	GSI, GS72116TP-12
1	ADM3311EARS	U16	Analog Devices, ADM3311EARS
1	MAX5251BEAP	U18	Maxim, MAX5251BEAP
1	PCA82C250T	U20	Philips Semiconductor, PCA82C250T
Resistors			
20	16K Ω	R1, R2, R6, R7, R9, R10, R16, R17, R20, R21, R24, R25, R28, R29, R67, R68, R108, R109, R111, R112	SMEC RC73L2A16KOHMJT
10	1M Ω	R3, R8, R11, R18, R22, R26, R30, R69, R110, R113	SMEC RC73L2A1MOHMJT
21	5.1K Ω	R4, R12, R13, R19, R23, R27, R31, R32, R35, R37, R41, R57, R70, R105, R106, R114, R115, R121, R122, R123, R126	SMEC RC73L2A5.1KOHMJT
11	10K Ω	R42, R43, R44, R46, R48, R49, R72, R73, R74, R119, R120	SMEC RC73L2A10KOHMJT

Qty	Description	Ref. Designators	Vendor Part #s
Resistors (Continued)			
2	51 Ω	R33, R34	SMEC RC73L2A51OHMJT
3	47K Ω	R36, R38, R104	SMEC RC73L2A47KOHMJT
1	470 Ω	R40	SMEC RC73L2A470OHMJT
1	10M Ω	R45	SMEC RC73L2A10MOHMJT
19	1K Ω	R50, R51, R52, R53, R55, R75, R78, R81, R84, R87, R90, R93, R96, R100, R101, R102	SMEC RC73L2A1KOHMJT
9	270 Ω	R58, R59, R60, R61, R62, R63, R64, R65, R66	SMEC RC73L2A270OHMJT
16	24 Ω	R76, R77, R79, R80, R82, R83, R85, R86, R88, R89, R91, R92, R94, R95, R97, R98	SMEC RC73L2A24OHMJT
1	120 Ω , 1/4W	R118	YAGEO CFR 120QBK
Potentioneters			
7	10K Ω	R5, R14, R15, R71, R107, R116, R117	BC/MEPCOPAL ST4B103CT
Inductors			
4	1.0mH	L1, L2, L3, L4	Fair-Rite 2743015112
LEDs			
1	Red LED	LED1	Hewlett-Packard HSMS-C650
4	Yellow LED	LED2, LED4, LED6, LED8	Hewlett-Packard HSMY-C650
5	Green LED	LED3, LED5, LED7, LED9, LED10	Hewlett-Packard HSMG-C650
Diode			
3	S2B-FM401	D1, D2, D3	Vishay DL4001DICT

Qty	Description	Ref. Designators	Vendor Part #s
Capacitors			
5	2.2 μ F, 50V DC	C1, C2, C23, C54, C60	NICHICON UWX1H2R2MCR2GB
49	0.1 μ F	C3, C4, C5, C6, C7, C8, C9, C10, C12, C14, C16, C17, C18, C19, C20, C21, C22, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C35, C38, C39, C40, C41, C44, C46, C47, C48, C49, C50, C51, C52, C53, C59, C65, C67, C68, C69, C70, C71, C72	SMEC MCCE104K2NR-T1
1	470 μ F, 16V DC	C11	PANASONIC ECE-V1CA471P
2	47 μ F, 10V DC	C13, C15	PANASONIC ECE-V1AA470P
8	470pF	C55, C56, C57, C58, C61, C62, C63, C64	SMEC MCCE471J2NO-T1
Jumpers			
9	3 x 1 Bergstick	JG1, JG2, JG6, JG11, JG15, JG16, J16, J17, J25	SAMTEC TSW-103-08-S-S
4	4 x 2 Bergstick	JG3, JG4, J4, J20	SAMTEC TSW-104-08-S-D
6	1 x 2 Bergstick	JG5, JG7, JG8, JG9, JG17, JG18	SAMTEC TSW-102-08-S-S
1	1 x 1 Bergstick	JG10	SAMTEC TSW-101-08-S-S
3	3 x 3 Bergstick	JG12, JG13, JG14	SAMTEC TSW-103-07-S-T
2	9 x 2 Bergstick	J1, J2	SAMTEC TSW-109-08-S-D
3	6 x 1 Bergstick	J3, J5, J6	SAMTEC TSW-106-08-S-S
5	5 x 2 Bergstick	J7, J9, J26, J28, J32	SAMTEC TSW-105-08-S-D
2	4 x 1 Bergstick	J8, J19	SAMTEC TSW-104-08-S-S
2	7 x 2 Bergstick	J29, J14	SAMTEC TSW-107-08-S-D
2	14 x 1 Bergstick	J21, J22	SAMTEC TSW-114-08-S-S
2	6 x 1 MTA	J23, J24	AMP MTA 640456-6
1	6 x 2 Bergstick	J27	SAMTEC TSW-106-08-S-D
2	20 x 2 Shrouded	J30, J31	3M 2540-6002UB

Qty	Description	Ref. Designators	Vendor Part #s
Test Points			
8	1 × 1 Bergstick	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8	Samtec TSW-101-08-S-S
Crystals			
1	8.00MHz Crystal	Y1	ECS-80-18-5P
Connectors			
1	DB25M Connector	P1	AMPHENOL 617-C025P-AJ121
1	2.1mm coax Power Connector	P2	Switch Craft RAPC-722
1	DE9F Connector	P3	AMPHENOL 617-C009S-AJ120
Switches			
5	SPST Pushbutton	S1, S2, S3, S4, S5	Panasonic EVQ-QS205K
1	SPDT Toggle	S6	C&K GT11MSCKE
Transistors			
1	2N2222A	Q1	ZETEX FMMT2222ACT
Miscellaneous			
27	Shunt	SH1–SH27	Samtec SNT-100-BL-T
6	Rubber Feet	RF1–RF6	3M SJ5018BLKC

INDEX

Numerics

16-bit 3.3V hybrid controller [2-1](#)
4.0Amp power supply [2-13](#)
4-Channel 10-bit Serial D/A [2-1](#)
56F805 Technical Data [Preface-x](#)
64Kx16 bits of data memory [2-1](#)
64Kx16 bits of program memory [2-1](#)
8.00MHz crystal oscillator [2-1](#)

A

A/D [Preface-ix](#)
Analog-to-Digital
 A/D [Preface-ix](#)

B

Back-EMF [2-23](#)

C

CAN [Preface-ix](#)
 bus termination [2-1](#)
 bypass [2-1](#)
 interface [2-1](#)
CAN in Automation
 CiA [Preface-ix](#)
CAN interface [2-1](#)
CAN physical layer peripheral [2-2](#)
CiA [Preface-ix](#)
Connector
 A/D [2-33](#)
 Address bus [2-32](#)
 CAN [2-35](#)
 Data bus [2-33](#)
 External Memory Control [2-29](#)
 PWM [2-36](#)
 SCI [2-34](#)
 SPI [2-35](#)
Connectors
 Peripheral Expansion [2-27](#)
Controller Area Network
 CAN [Preface-ix](#)

D

D/A [Preface-ix](#)
D/A converter [2-18](#)
Data memory [2-4](#)
Debugging [2-7](#)
Development Card [2-1](#)
Digital-to-Audio
 D/A [Preface-ix](#)
DSP56800 Family Manual [Preface-x](#)
DSP56F801/803/805/807 User's Manual [Preface-x](#)

E

Encoder/Hall-Effect [2-24](#)
 circuits [2-24](#)
Encoder/Timer [2-30](#)
Evaluation Module
 EVM [Preface-ix](#)
EVM [Preface-ix](#)
External Memory Control Signal [2-29](#)
external memory expansion connectors [2-2](#)
external oscillator frequency input [2-1](#)

F

FSRAM [2-1](#), [2-4](#)

G

General Purpose Input and Output
 GPIO [Preface-ix](#)
GPIO [Preface-ix](#), [2-27](#), [2-32](#)
 signals [2-17](#)

H

Hall-Effect/Quadrature Encoder interface [2-1](#)
Host Parallel Interface Connector [2-7](#)
Host Target Interface [2-7](#)

I

IC [Preface-ix](#)
Integrated Circuit
IC [Preface-ix](#)

J

Joint Test Action Group
JTAG [Preface-ix](#)
JTAG [Preface-ix](#), 1-1, 2-1
connector 2-8
JTAG port interface 2-1
Jumper Group 1-3
JG1 1-3
JG10 1-4
JG11 1-4
JG12 1-4
JG13 1-4
JG14 1-4
JG15 1-4
JG16 1-4
JG17 1-4
JG18 1-4
JG2 1-3
JG3 1-3
JG4 1-3
JG5 1-3
JG6 1-3
JG7 1-3
JG8 1-3
JG9 1-3

L

Logic
motor bus over-current 2-1
motor bus over-voltage 2-1
motor zero crossing 2-1
Low-Profile Quad Flat Pack
LQFP [Preface-ix](#)
LQFP [Preface-ix](#)

M

motor bus
over-current 2-1
over-voltage 2-1
Motor Phase Current 2-23
Motor Protection Logic 2-19
MPIO [Preface-ix](#), 2-28, 2-30
port 2-30, 2-31
MPIO-compatible peripheral 2-1, 2-2
Multi Purpose Input and Output
MPIO [Preface-ix](#)

O

On-board power regulation 2-2
OnCE [Preface-ix](#)
OnCE(TM) 1-1
On-Chip Emulation
OnCE [Preface-ix](#)

P

Parallel JTAG Host Target Interface 2-1
PCB [Preface-ix](#)
Phase Locked Loop
PLL [Preface-ix](#)
PLL [Preface-ix](#)
Printed Circuit Board
PCB [Preface-ix](#)
Program memory 2-4
Pulse Width Modulation
PWM [Preface-ix](#)
PWM [Preface-ix](#)
PWM-compatible peripheral 2-2

Q

Quad Encoder 2-24
Quadrature Decoder
interface port 2-29

R

- RAM [Preface-ix](#)
- Random Access Memory
 - RAM [Preface-ix](#)
- Read-Only Memory
 - ROM [Preface-ix](#)
- real-time debugging [2-7](#)
- ROM [Preface-ix](#)
- RS-232
 - interface [2-5](#)
 - level converter [2-5](#)
 - schematic diagram [2-5](#)
- RS-232 interface [2-1](#)

S

- SCI [Preface-ix](#)
 - Serial Communications Port [2-34](#)
- Serial Communications Interface
 - SCI [Preface-ix](#)
- Serial Peripheral Interface
 - SPI [Preface-ix](#)
- SPI [Preface-ix](#)
 - Serial Peripheral Interface [2-35](#)
- SPI-compatible peripheral [2-1](#)
- SRAM [Preface-ix](#)
 - external data [2-1](#)
 - external program [2-1](#)
- Static Random Access Memory
 - SRAM [Preface-ix](#)

T

- Timer-compatible peripheral [2-2](#)

U

- UART [Preface-ix](#)
- UNI-3
 - Back-EMF [2-23](#)
 - connector/interface [2-14](#)
 - DC Bus Over-Voltage signal [2-20](#)
 - Motor Drive interface [2-15](#)
 - Motor interface
 - Primary [2-2](#)
 - Secondary [2-3](#)
 - Over-Voltage signal [2-21](#)
 - Unattached Signal Connector [2-38](#)
- Universal Asynchronous Receiver/Transmitter
 - UART [Preface-ix](#)

Z

- Zero-Crossing
 - circuits [2-24](#)
- Zero-Crossing Detection [2-24](#)

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